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Hardware designer's compendium

The Printed Circuit Board 2010

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The third dimension of the PCB
Page 16 **Benefits of Metallizing PCB Edge**

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The Printed Circuit Board 2010



Claudia Mallok

"The Printed Circuit Board 2010" continues the successful article series "The Printed Circuit Board 2005" which set a new standard in 2003/2004. "The Printed Circuit Board 2010" also stands for a holistic view of electronics and its implementations: from the selection of components, a design that is compliant with EMC regulations and physically suitable, to the producibility of the printed circuit board and the assembling of the module.

The meltemi board is in the focus of our reporting – an application platform designed for transmission bandwidths of up to 60 Gbit/s in HDTV applications, image processing or fast data multiplexers. It implements an intense consideration of signal integrity, fast data transfer via LVDS, an extreme EMC specification and the capacitive use of power planes. The printed circuit board for meltemi features 20 layers, a multi-power system, a stapled power supply in multiple adjacent layers, with 50 µm line spacing, plugged vias and metallized edge.

Reference design for stable high speed boards presented by experts

In 14 chapters, the partners involved in this project describe the development of the meltemi module, from component selection down to EMC tests in the measurement lab. Experts give decision aids and describe approaches towards a promising solution for board hardware stability under such challenging circumstances. On pages 62–79, we also supply the articles from the preceding series which are often referred to by the authors.

The meltemi project has shown that the design of complex modules is a real challenge for developers. They have to implement the latest module technology progress and the facilities of PCB production and layout on a CAD system. The project has also demonstrated the need for partnership and joint approaches to a progressive project in which the requirements from all departments involved are considered – a prerequisite for the development of functionally optimized modules according to a holistic view of electronics.

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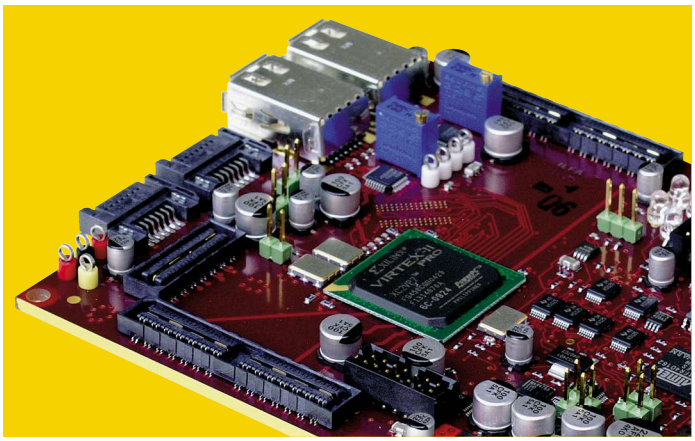
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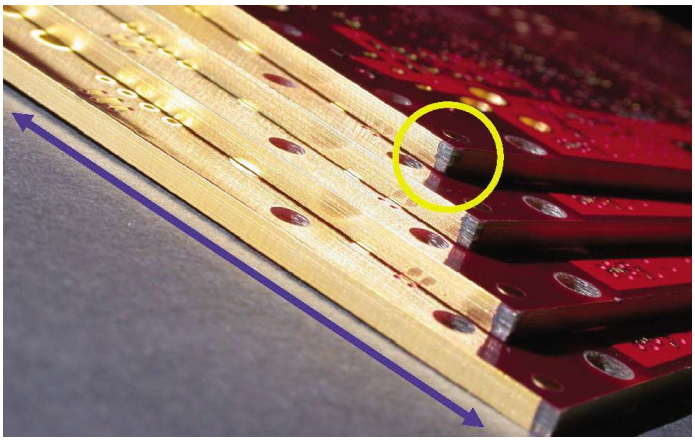
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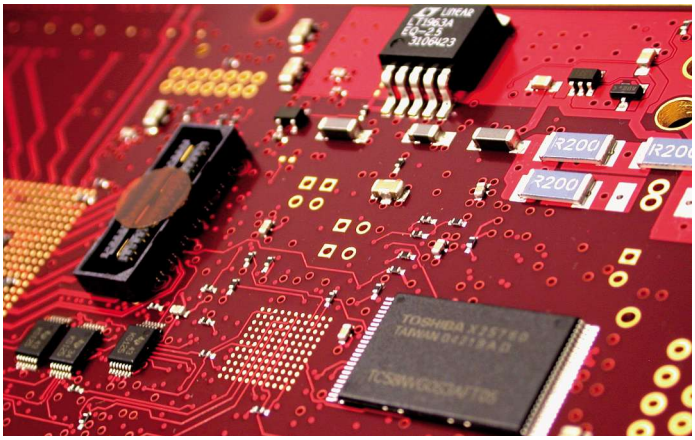
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Serial high speed data transfer
The "meltemi"-platform is designed for a field where loads of data have to transmitted. The first part of this project concentrates on the serial transceivers and the consequences for their environment in respect to emission and the fuctional stability of the module. **Page 6**

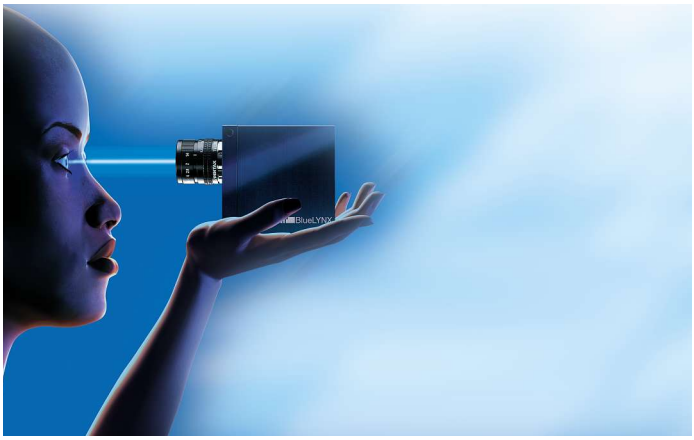


Revolutionised physical properties of electronic devices
One speciality of the PCB for the application platform meltemi is the edge plating. Edge plating provides clear measurable advantages at comparably ignorable costs for devices with demands regarding EMC, signal-integrity and de-heating. The third dimension of PCB is described in chapter 3. **Page 19**





Terminating powerplane systems
Design engineers who implement powerplane systems as multi-dimensional lines will discover a wealth of benefits for decoupling and EMC. This way requires appropriate countermeasures in order to maintain solid power integrity and sound EMC characteristics. **Page 47**



Realtime processing of complex imaging formats
Due to their structure FPGAs are perfectly suited to solve tasks in two dimensional signal processing. The combination of FPGA and suitable microprocessor has significant speed-ups especaily concerning realtime image processing. **Page 59**

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The Consequences of serial Transceiver

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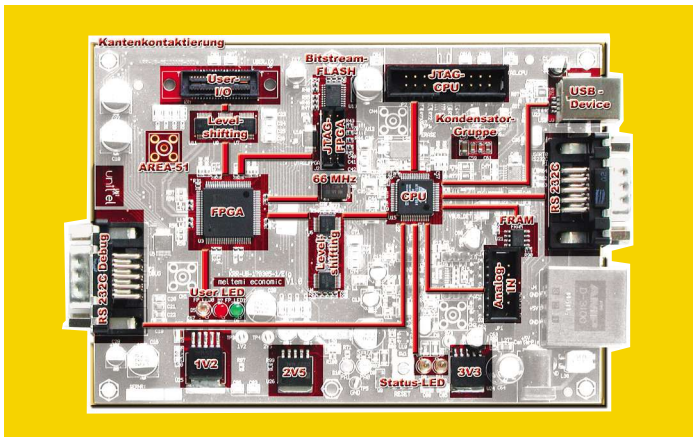
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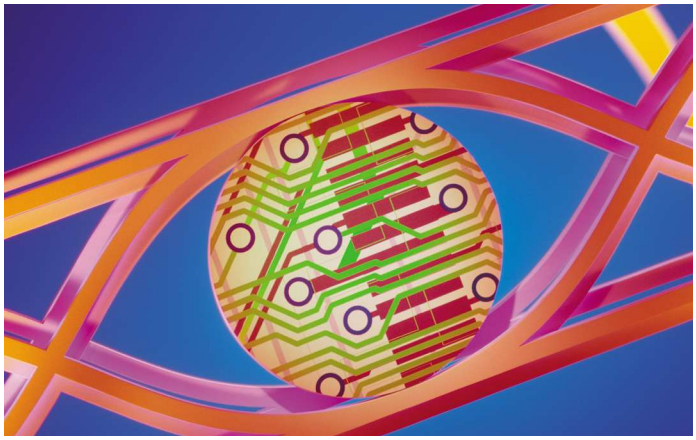
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The Edge Capacitor

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Squaring the circle
The latest task was, to project the experience gained with high density multi-layer boards from the 20 layer level towards the 6 layer level without loosing too much in respect to EMC behaviour and stable functionality. The common operating strategies for future circuits are shown in chapter 6. **Page 36**





EMC-compliant microprocessor board design
EMI and fuctional stability of a system are linked in a way, what without profound EMI measures system stability and fuction cannot be achieved. The EMC-conform design of a microprocessor board is divided into three areas of provisions. **Page 76**

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Quiet, please!

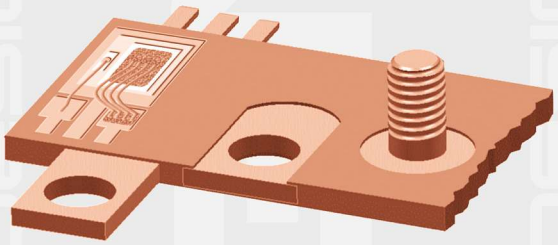
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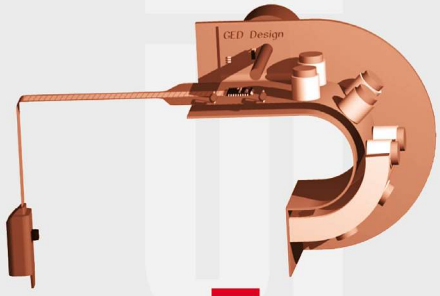
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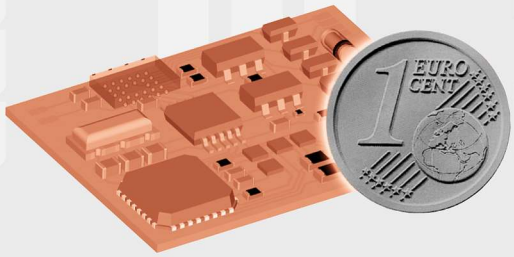
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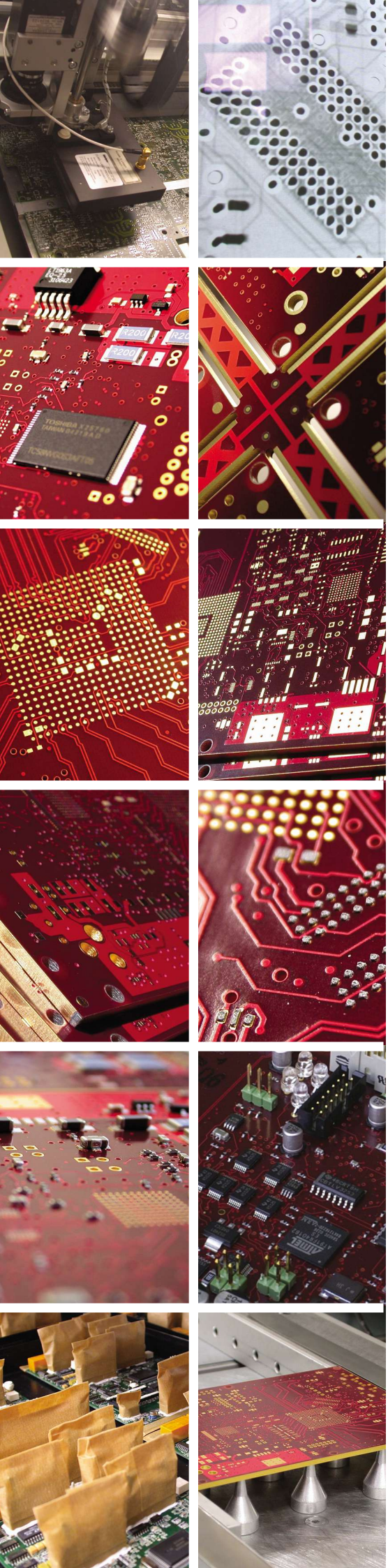


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Chapter 1

Serial high speed data transfer

The Consequences of Transceiver

Highly integrated transceiver-technology makes it feasible: instead of 400 or 600 Mbit/s per LVDS channel use 2.5 Gbit/s (5 Gbit/s full duplex) as serial data transfer rate per CML channel now. Some people think, that the up to now used moderate transfer rates will be sufficient in the future. Nevertheless they will not escape from dealing with high speed technologies. Reasons can be found in the involved speedy signal slopes and the associated introduction of noise through the power supply pins of the high speed devices. The first part concentrates on the serial transceivers in the application platform "meltemi" and the consequences for their environment in respect to emission and the functional stability of the module.

by Gerhard Eigelsreiter

The old Greeks already knew "Etesien" (derived from "etos"- cyclically every year) , Meltemi, the wind of beautiful weather, which comes from the north and can be experienced as relaxing cool breeze during hot summer days. Its origin is located in the northern Aegean see. All the time beautiful weather and a nice clear view are its special attributes. A clear and nice view is also necessary for everyone, who wants to go into the advanced fields of serial high speed data transfer with rates in the multi gigabit range with respect to hardware. In order not to loose the good clear view, the name "meltemi" was chosen to stand as godfather for the hardware to be described in this series of articles "the PCB 2010".
It was the declared goal in this series to spotlight some development projects of that kind, to give some help in the decision making process and to describe alternatives, which indicate a promising path out of a labyrinth of solution probabilities towards a stable board level hardware.
The central point of the meltemi board is an FPGA with integrated serial transceivers, with fix wired support logic and with a 32 bit single chip microcontroller (Figure 1). The I/O Ports through the FPGA towards the peripherals are generally realised using balanced signal interconnects. From the available 77 differential channels 61 channels support 600 Mbit/s each, the agglomerate total transfer rate via these channels shows to be 36 Gbit/s on these channels. For the remaining 16 channels eight integrated 2.5 Gbit/s transceivers (with a total of 40 Gbit/s) are implemented.

77 differential channels and 61 LVDS line pairs

Four of these transceivers can communicate with the outer world via two Infiniband- and two Serial ATA connectors. The remaining 4 transceivers as well as the 61 LVDS line pairs use 4 impedance defined high speed connectors, which form extensions for plug on boards.
The two Infiniband connectors are not directly coupled with the transceivers: the secure and problem free physical data transfer over larger distances (up to 17 meters) is granted through adaptive cable drivers and equalizers. Everyone who asks himself, for which applications such gigantic transfer rates may be used, only has to throw a look onto the letter

to Santa Claus of his current or potential future customers within the next years. Good for these, for whom moderate data transfer rates will be sufficient within the coming years. This does not save the lucky ones from fast signal transients and from noise introduction through the power supply pins of his chips. There do not seem to be boarders with the fantasies of chip manufacturers to scan the limits of semiconductor physics and to reach beyond limits.

The consequences of serial transceivers on their environment

Topics within our contribution are serial transceivers with the inevitable consequences towards their environment in respect to EM emission and towards their influence on the stability of the remaining (environmental) hardware. Focus is a comparison of various measurements in the near- and far-field for two different cable-connector pairings: considered will be Infiniband as high quality solution as well as Serial ATA as economic, PC associated variant. In both cases the total physical channel transfer rate is 2.5 Gbit/s, full duplex.
For the link layer protocol "Aurora" from Xilinx was used.
This is a protocol for point-to-point interconnects, which can be handled fairly easy. For measurements in the near field a H-field sensor form our partner Dirks Corporate Consulting was used (see page 80).
Results from far field measurements performed at the TGM Institute of Technology EMC facilities were used to verify the Lab results. The results "meltemi" with Infiniband (I1 to I6) and Serial-ATA (S1 to S6) board to board cable interconnects are summarized on page 10.
The cable length in the Infiniband-case is 10 meters, for Serial-ATA it is 1 meter. The measurements were performed with (I1 to I3, S1 to S3) and without user data load (I4 to I6, S4 to S6). For the measurement areas with the H-field sensor (I1, I4; S1, S4) the SMD Pads of the corresponding connector on the PCB and the transitional zones between cable connector and actual beginning of the cable (I2, I6; S3, S6) were chosen. The representation as well as the storage of acquired time domain data (I2, I5; S2, S5) was done using the 6 GHz Scope WaveMaster 8600A (LeCroy). Evaluation of these curves shows considerable differences between Infiniband- and Serial-ATA Connectors in respect to EM emission. Although a 10 meter cable had been used and additional adaptive cable-equalisers in the case of Infiniband, no significant emission levels can be identified, neither in near field (I1, I4, I3, I6) nor in the EMC Lab (I7, using a 10 m and I8 using a 3 m Infiniband Interconnect Cable).

The correctly designed and decoupled power supply system works

With a Serial-ATA-Interconnect (considering only short connection distances of 1 m and below) , both in the Near Field (S1,S4, S3, S6) as well as in the EMC emission lab (S8: 1 m cable and S7: 5 cm cable) the situation looks much worse. Only at very short distances (5 cm) with the Serial ATA Interconnect, the Emission levels drop to an acceptable magnitude. Responsible for this effect are massive impedance mismatchings and the unappropriate screening of the Serial ATA-Connector-Cable Assembly. Using Ferrite Cores, which can be applied to the cable, part of the emission can be reduced. And this possibility works only due to our broadband Power supply decoupling system with its stacked power supply planes.



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As it can be seen from measurement S7 (taken in the EMC lab) the emission levels shrink clearly below SATA cable lengths of about 5 cm and subsequently reach Infiniband emission performance. This is a clear proof for the superiority of PCBs with a correctly designed and decoupled power supply system. Addendum to the images I1, I3, I4, I6 concerning the Infiniband Cable Interconnect:
Here we are not showing space-wasting copies of one and the same measurement. There was simply nothing to measure at all in terms of emission.
The single spikes are rather the residues of external sources such as mobile phone masts. From the author's view and specially from the viewpoint of the reader a disappointing graphic representation, which can only cause boredom. The conclusion, that the serial ATA interconnects with their refreshing lively EMC performance were only chosen to show a good contrast and as justification for this comparison, is without any foundation.

On the other hand, in order to generate attention of the reader, the author thankfully accepts this case.
Which hints can be read out of the Diagrams (S1, S4, S3, S6)?
Which useful details can be filtered out?
First the disappointing conclusion, that without user data transport (S4, S6, from the viewpoint of the user nothing at all should be transferred) the emission figures reach a maximum at the 1.25 GHz Base frequency. This can be argued by the fact, that normally this base frequency is needed for the synchronisation of the FPGA Transceiver Receiver-specific hardware, in order not to show unacceptable long resynchronisation periods. If one is not lucky, this situation may lead to a EMC emission violation and the EMC test fails through merely "doing nothing" (no User Data).

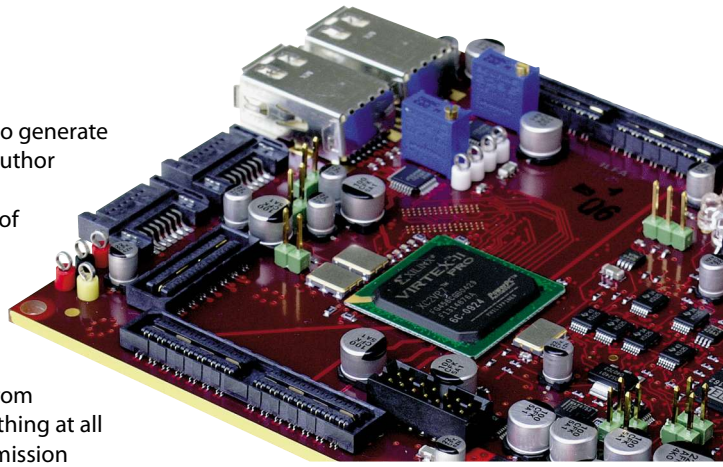
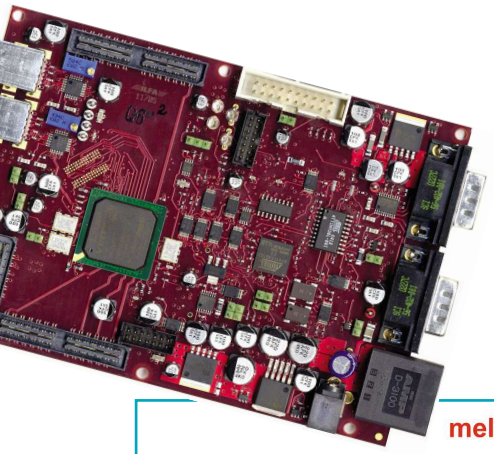
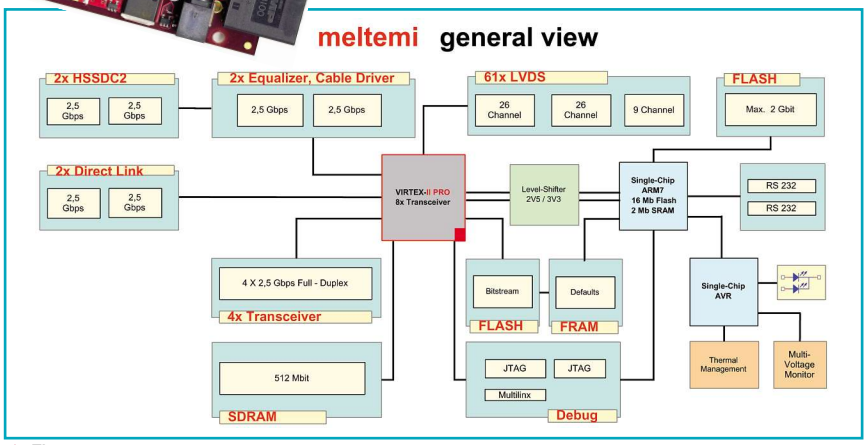


Figure 3:
meltemi transceiver solution without a garden fence:
Instead of chokes capacitors and connection lines, areal, broadband decoupled supply planes are integrated within the PCB.
Result: much space available for signal lines.

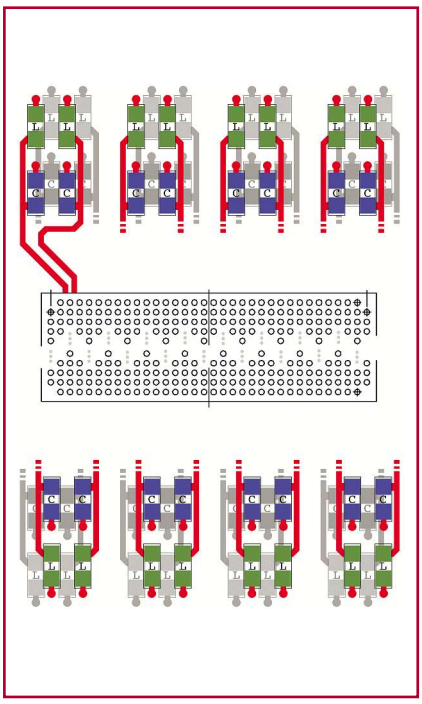
Carefully consider cost and yield of cable interconnects

Some hardware developers state, claiming, that most boards tested do not contain FPGAs and serial high speed transceivers at all, that the above mentioned effect actually would be the cause for the high count of repetitive EMC tests. The author strictly does not share this sort of sarcasm at all. Using cable interconnect techniques for transfer rates in the multi Gigabit range, specially in the industrial environment, it is mandatory to carefully look at the trade off between cost and performance. Looking at the serial ATA interconnect with its significant higher emission levels forces the hardware designer to study comprehensively solution approaches within many technology areas, which will be cross-connected in the future. This is a contradiction to the current global market doctrine, to develop more and more powerful hardware suitable for series production within decreasing time spans and to position the hardware in due time in marketing windows. Long termed co operations and partnerships show to be increasingly ▶

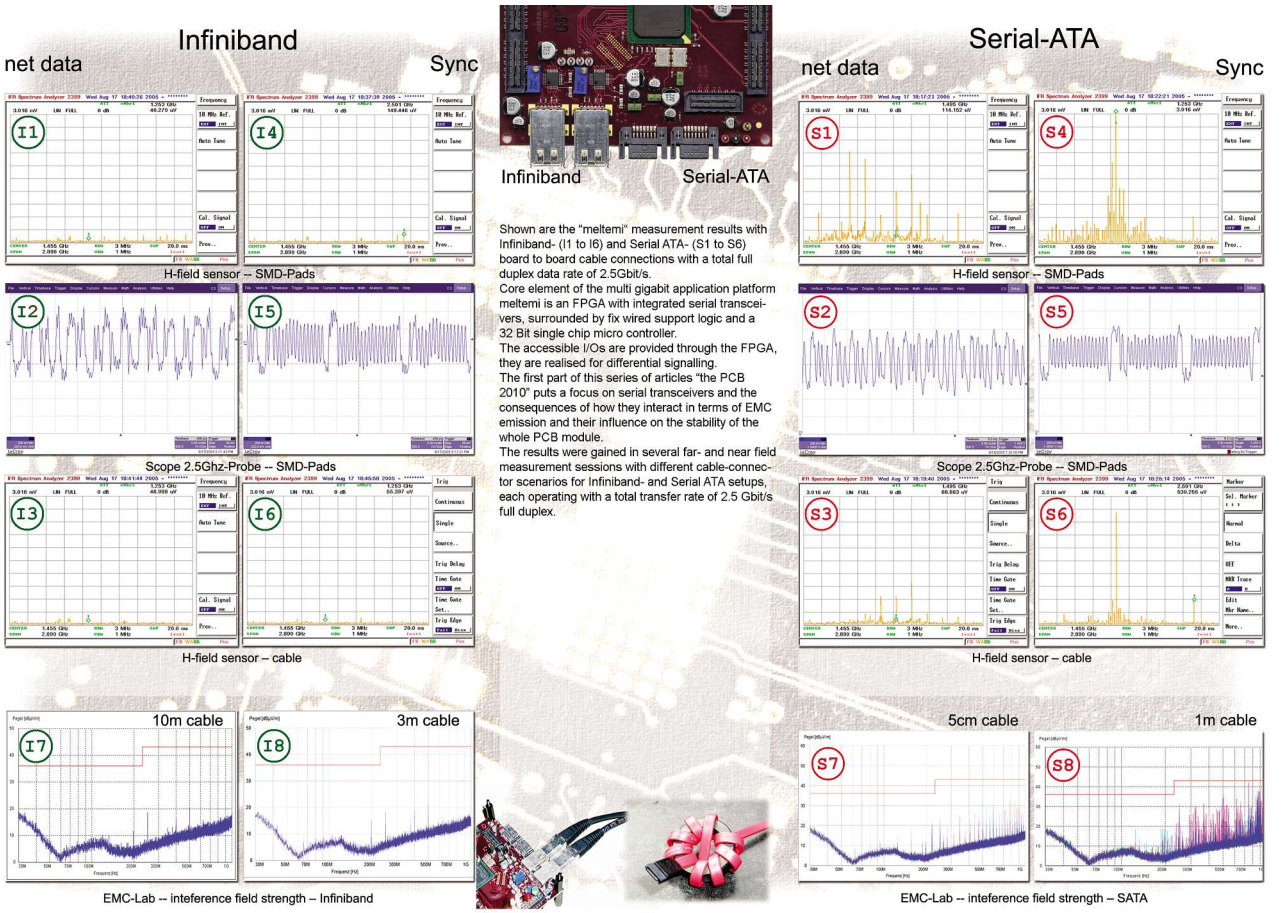




▲ Figure 1:
meltemi board: block diagram and assembled board
Central device on the meltemi board is an FPGA with integrated serial transceivers, surrounded by fix wired support logic and a 32 bit single chip microcontroller.



▶ Figure 2:
Garden fence for 8 transceivers on the PCB top- and bottom layers. The FPGA is only partially drawn. A challenge for every pcb designer. The results in respect to improvements of signal integrity to grant stable and error free communications are very poor.



Shown are the "meltemi" measurement results with Infiniband- (I1 to I6) and Serial ATA- (S1 to S6) board to board cable connections with a total full duplex data rate of 2.5Gbit/s.
Core element of the multi gigabit application platform meltemi is an FPGA with integrated serial transceivers, surrounded by fix wired support logic and a 32 Bit single chip micro controller.
The accessible I/Os are provided through the FPGA, they are realised for differential signalling.
The first part of this series of articles "the PCB 2010" puts a focus on serial transceivers and the consequences of how they interact in terms of EMC emission and their influence on the stability of the whole PCB module.
The results were gained in several far- and near field measurement sessions with different cable-connector scenarios for Infiniband- and Serial ATA setups, each operating with a total transfer rate of 2.5 Gbit/s full duplex.

important, specially as R&D demands grow significantly.
Garden fences and other calamities developers, active in the arena of high speed interconnects, i.e. in the near future all, who implement FPGAs with fast serial transceivers on a PCB, will have thrown a suspicious glimpse on the strange choke-capacitor constructs for the decoupling of the transceiver supply pins. With 8 transceivers, one still needs 32 chokes and the same amount of capacitors (figure 2).
But the very impression garden fences result with 24 transceivers. For every PCB designer this means a horror scenario in respect to placement, compliance with design rules for differential signal lines and a multitude of further measures for the improvement of signal integrity to reach a stable and as far as possible distortion free data communications.
The expenditure to achieve all this is overwhelming. The result mostly ranges from poor to not usable. This is, because the necessary broadband decoupling measures simply have not been considered. Nevertheless the garden fence approach is mandatory demanded – not just proposed – in data sheets and application notes.
What does the originator of the problems, the semiconductor manufacturer, offer in addition? Besides some seldom exceptions the good old support capacitor approach, mostly using 100 nF SMD capacitors. With the expected high switching frequencies the effect of such a support capacitor exactly and practically can be described with zero, an easily applicable rule of the thumb.
That means: much support can not be expected. It would be more intelligent, to scrap these garden fences at all (s. figure 3). (Note: there exist proposals, where they would again be necessary, but in these cases they have an effect).
It is not so simple, only just to leave out the garden fences, because these constructs are not demanded from the PCB designers without reason.
Using a sort of barter the requirements set by the laws of physics can be satisfied: Instead of using huge amounts of chokes, capacitors and conductors, areal supply layers, intelligently decoupled by capacitor groups to form a broadband decoupled supply system, are integrated in a certain geometry within the multilayer PCB.
In the application board "meltemi" such a layered construct was realised and the board performance was critically tested. The results were superb, in respect to the near field emission and the far field emission. With the Infiniband connector-cable combination no transmission errors were detectable at transfer rates of 2.5 Gbit/s over 10 meters. The same was true with 2 channels operated in parallel, i.e. 5 Gbit/s. Our partner and PCB manufacturer ILFA undertook the necessary research for the producability of the board.

References:

RocketIO™ Transceiver User Guide UG024 (v2.5) December 9, 2004, Virtex-II Pro, Xilinx,
Virtex-II Pro and Virtex-II Pro X FPGA User Guide UG012 (v3.0), August 2004, Virtex-II Pro, Xilinx
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Chapter 2

Routing of differential high speed signal lines

Watch High Speed PCB Design Rules

Modern EDA software offers many helpful assistants to ease the way for a 100% routing result. Does this result fulfil the physical conditions of the hardware in respect to functional stability and EMC requirements?
In fact, one does not reach the expected results without further deep reaching manual optimisations. In the second part of sour series of articles the developer describes, which set of measures is needed to reach a high degree of hardware stability in high speed applications and which proceedings have proved to be rewarding with the layout and routing of differential high speed signal lines.

by Gerhard Eigelsreiter

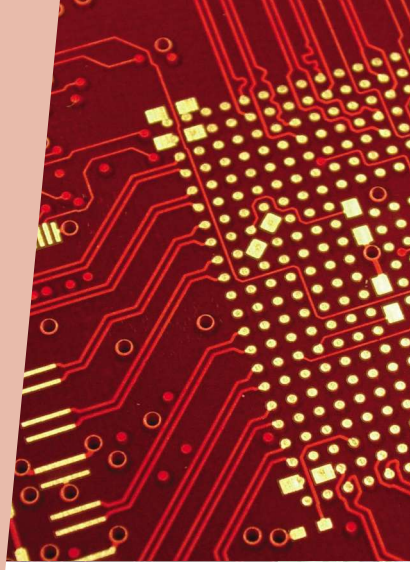
Referring to a PCB construct, the detailed visualisation of an imagined image commonly is termed "layout". The extension to the verbal monster "printed circuit board layout" or PCB layout nearly seems to be familiar compared to its decompressed version: "For the carrying devices of electronic components there is the necessity, in respect to establish production data, to transform the connection lines between active and passive electronic components into geometric pattern, which has to be applied to a printed circuit." Complicated and subtle as this formulation is the handling of many PCB layout software tools. At all corners helpful assistants are waiting to offer their help for a 100% routing result. But does this result fulfil the physical constraints of the hardware in respect to a good functional stability ant to good EMC results? In fact, one does not reach the expected results without manually performed optimisations.

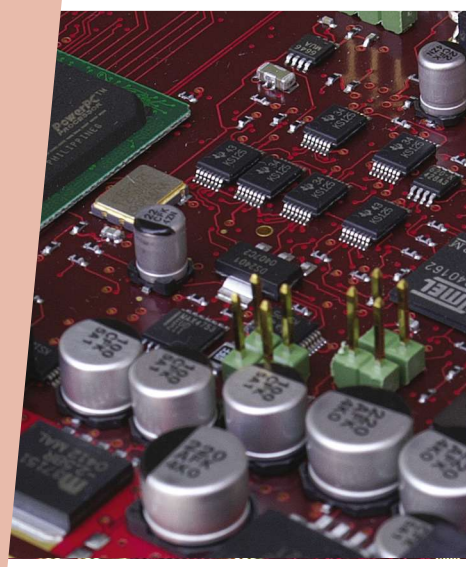
Ship around the software- and tolling riffs

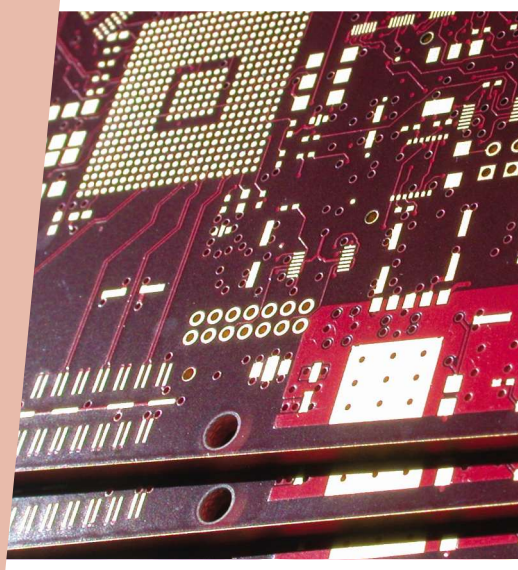
The imagined image of the solution, a very clear image per se, struggles, not to go lost within the considerations and tricks, which have to be applied to ship around the software- and tooling riffs and to cope with the Software assistants, available in huge quantities, but rarely equipped with the "disable" attribute. Layout tool producers claim, that the enormous complexity and consequently the sensitivity to errors was caused by the requirements of the users to target something like a push button design.

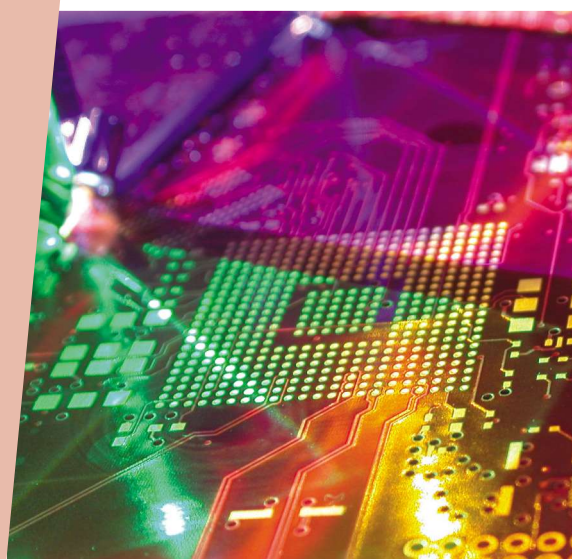
Form an interdiscilpinary contellation of specialist

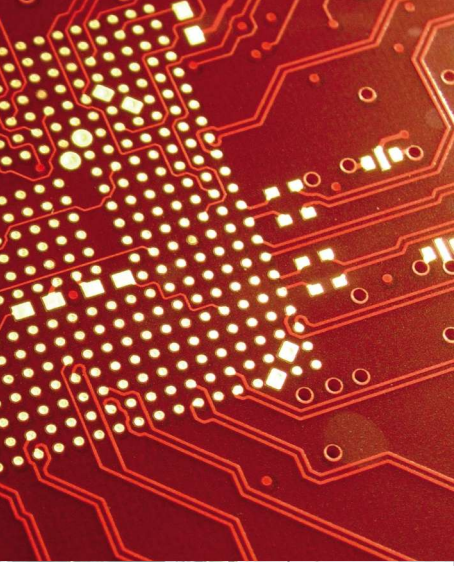
With ever reducing product cycle times, this goal seems further away than ever. Due to timing and commercial interests it is not sufficient any more, to outsource some minor project segments. It is now necessary to form a drastically augmented interdisciplinary constellation of specialists, producers and service suppliers. A group, which spans the track from basic sciences up to the production cycle in a close loop. A group, which is able and willing to provide this know how in every phase of the product development in the form of seminars conforming with practical requirements, with accompanying consulting or through complete and comprehensive hardware development.

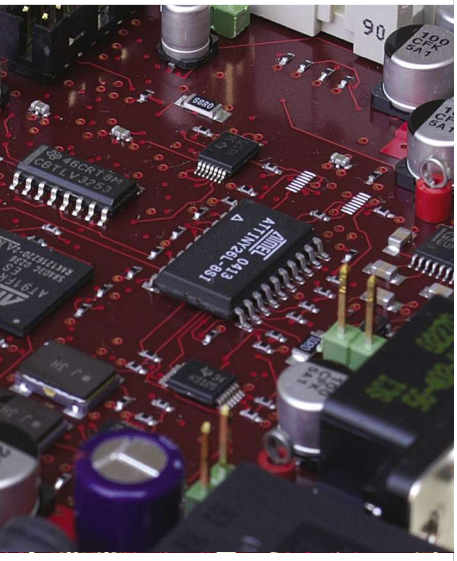


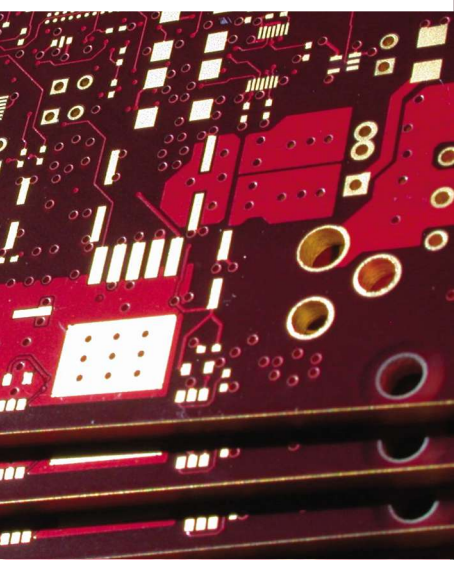


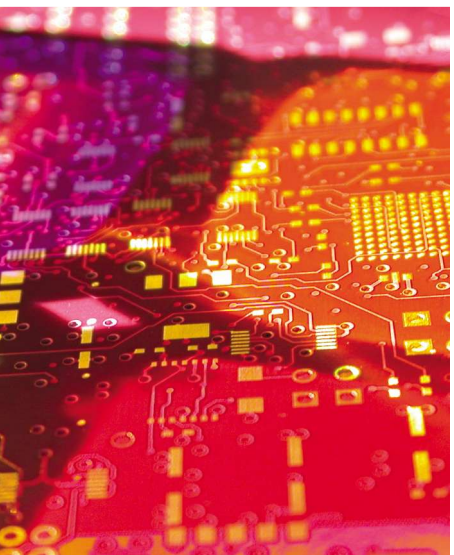










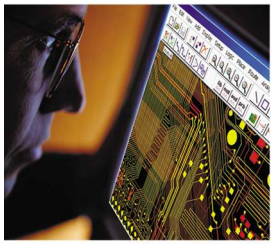


Who expects absolute perfection in all disciplines, will be disappointed immediately.
The R&D requirement could not be justified due to the enormous amount of time to be invested and it can not be justified, due to commercial reasons. Nevertheless a high degree in hardware stability can be reached in high speed applications and the therefore necessary solution approaches can be procured.
The stepchild "PCB Layout- and Production" is covered intensively through contributions by our partners within the coming articles.

A look at current PCB layouts shows, that still the major part of PCBs is realised using unsymmetric (single ended) signal lines for the transport of high speed signals. An increasing amount of associated problems in the respect of signal integrity, specially ground bouncing effects are negative symptoms. In the signal line, the current path from source to sink on the one hand gets all the attention, the return path (ground or ground lines) is often neglected in the PCB design.
The consequences are increasing instabilities ▶

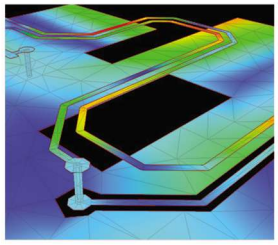
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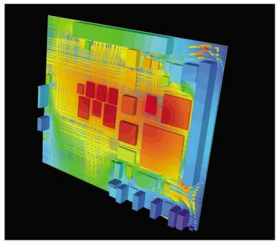


EMC / EMI

SimLab SoftwareGmbH

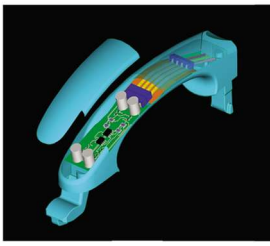
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and functional distortion within the PCB hardware. This situation is specially true for the broadband power supply decoupling, which is meanwhile inseparably coupled with stable system functionality.

Differential signalling demand comprehensive changes compared to traditional methods

What are the causes, which stand against a "change of paradigms" long overdue, a change from single ended signalling toward balanced signal lines? On the logical level there is no reason. One could think, let's go, let's start with balanced signalling. Layouters, suffering from experience will refuse at this point. And indeed, the suspicion is more than rectified. Differential signalling is accompanied by a legion of rules and measures, which demand comprehensive changes compared to traditional solution methods. This problem has been identified by EDA tool manufacturers as well, and they react through additional functions and options in their software updates. Nevertheless there is still too much space left for interactive interference. An excerpt of necessary measures and rules to be followed shall bring a little more light into the dark.

1) LDVS (Low Voltage Differential Signalling) requires to signal paths to be realised plane-parallel or sometimes above each other in certain distances which have to be determined in advance. The distances have to correlate with the desired termination impedance (e.g.100 Ω).
2) Depending on the transfer speed, the length differences within the differential pair shall not increase certain limits. Up to 1 Gbit/s the length difference should be less than 0.5 mm. PCIe requires at 2.5 Gbit/s maximal length differences of 0.1 mm!

Impedance changes within the signal lines hold be avoided or should be minimized

3) Impedance changes within the signal lines hold be avoided or should be minimized. Inevitable layer changes should be solved with the use of symmetrical via pairs. Ideally via pairs with only a moderate impedance change shall be applied (impedance defined vias). To determine the geometric values of the additional GND vias adequate software and simulation tools have to be used.
4) The distances between differential signal pairs should show at least the 5 fold value compared to the distance within the

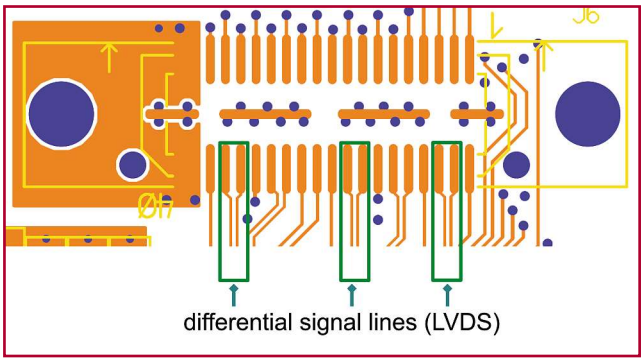


Figure 1:
shows the realisation of balanced and single ended signal lines, which are all brought across a 50 Ω (in respect to GND) connector

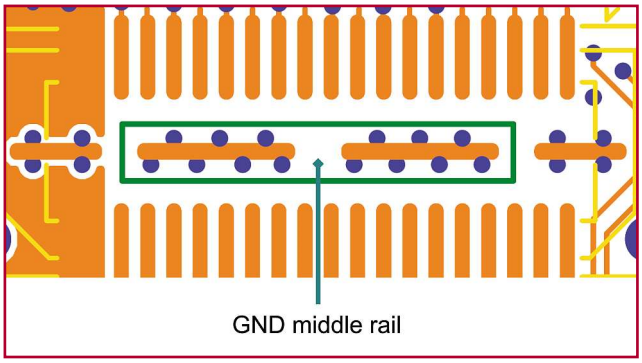


Figure 2:
The pads (in the green rectangle) of the GND rail of this connector construct are connected through several vias (blue spots) to the inner layer GND area. Slot-formation through too tightly positioned GND Vias have to be prevent at any cost.

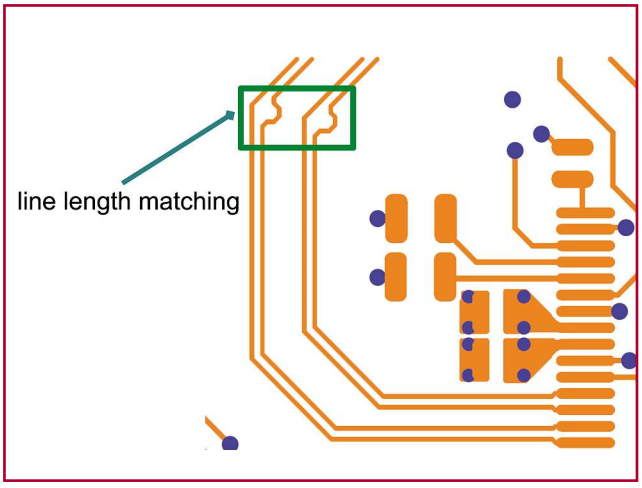


Figure 3:
Layout example for the signal line length matching (green rectangle) of differential pairs. At very fast signal rates (several Gbit/s) this matching has to be performed in a segmented fashion.

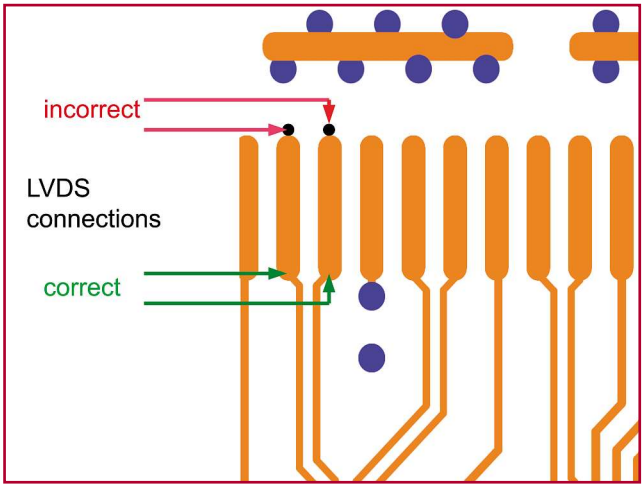
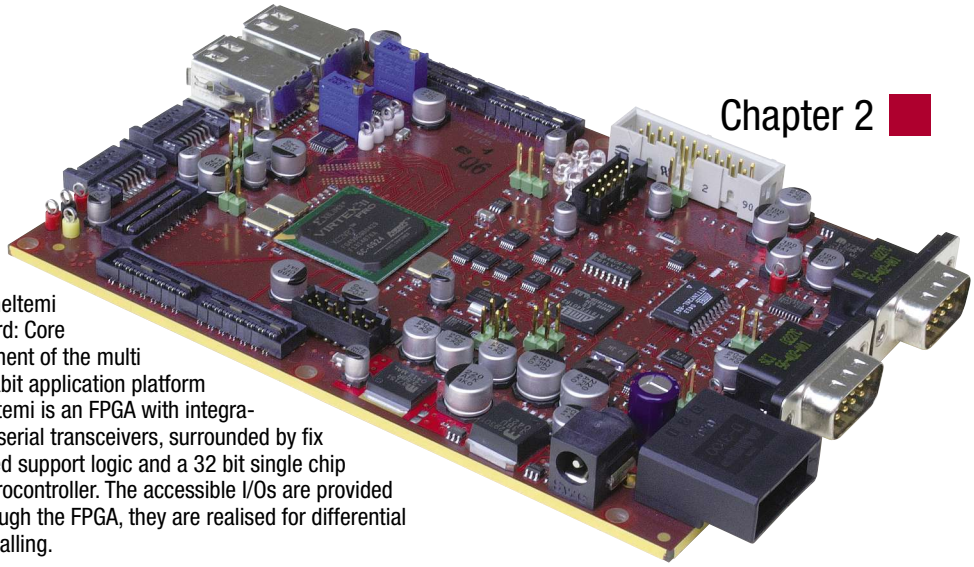


Figure 4:
For the elimination of line stubs the line has to be connected on the correct pad side. Here is an example showing the QSE-020-01-L-D-A from Samtec.

differential pair to minimize impedance distortion and cross talk. This is also true for neighbouring single ended lines.
5) The filling of free spaces with GND potential areas has an impedance distorting effect and should not be performed.
As an argument against differential methods often the requirement of the double amount of signal lines is quoted. This argument is in so far problematic, as the major rule "the return current is to be conducted as close as possible beside the forward current" had already been fully ignored in the past, in the TTL- as well as in the CMOS single sided signalling era.
To formulate it more precisely: The return current line was fully absorbed through the GND symbol in the schematic diagram. In the layout it was realised as inconvenient GND line or at the best as half hearted GND layer with many slots. THERE IS NOTHING LIKE A GND LAYER OR A GND LINE with the IDEAL IMEDANCE of 0 Ω!
Therefore the expressions as GND or GND-Area have to be replaced by the term "Signal Return Line" as fast as possible, if one wants to have at least a slight chance to pass the EMC test in the future, not to speak about stable hardware functionality.
Advantages of differential signalling are, besides high noise immunity and low signal voltages (about 350 mV with LVDS) specially the nearly complete absence of Ground Bouncing effects as well as very high potential transfer rates (>10 Gbit/s). As disadvantages the momentary big layout expense due to a complex design rule set and the application of interactive routing strategies has to be mentioned. The support through adequate tools lags far, in many cases in a non tolerable fashion, behind current requirements. *(cm)* ■



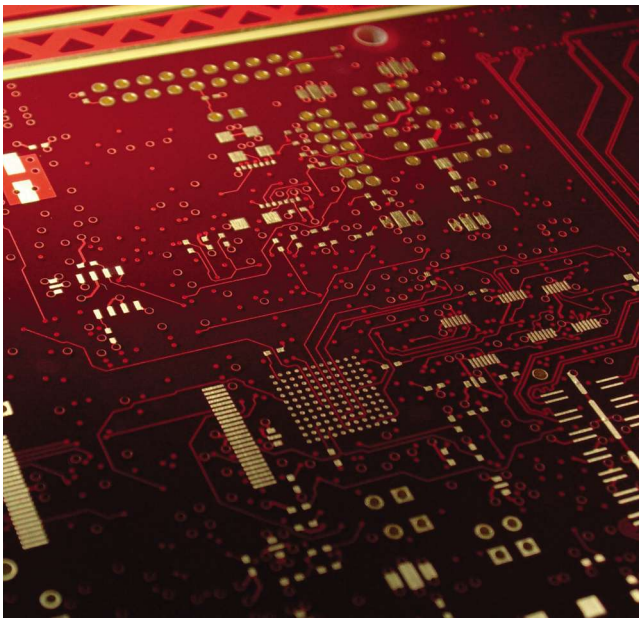
■ meltemi board: Core element of the multi gigabit application platform meltemi is an FPGA with integrated serial transceivers, surrounded by fix wired support logic and a 32 bit single chip microcontroller. The accessible I/Os are provided through the FPGA, they are realised for differential signalling.

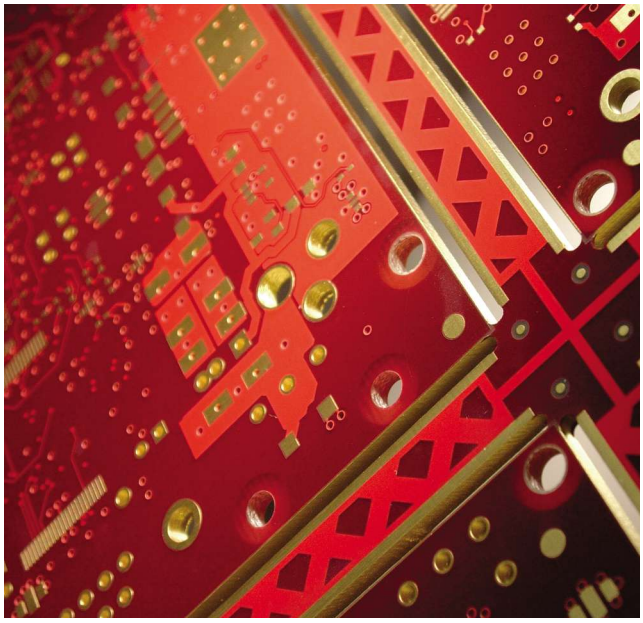


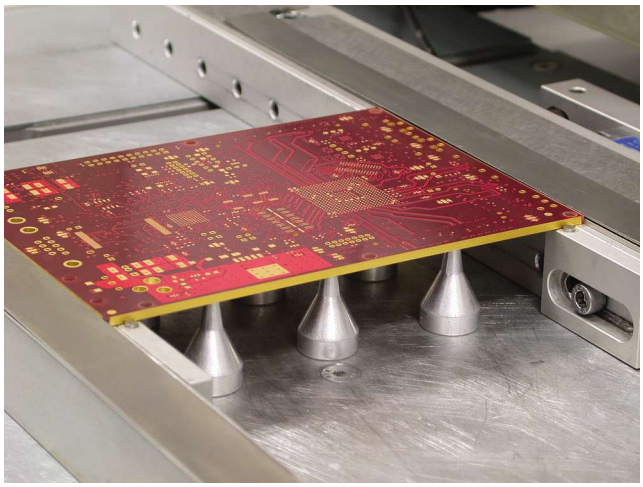
Chapter 3

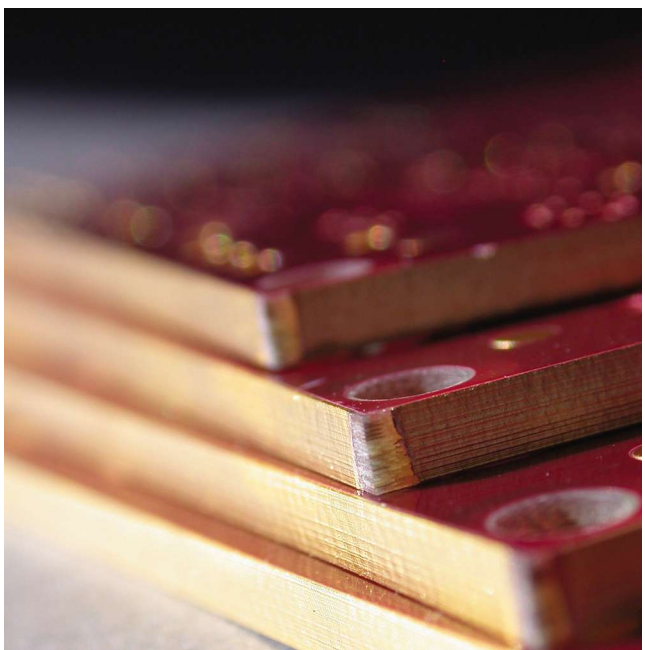
Revolutionised physical properties of electronic devices

Metallizing PCB Edges









One speciality of the PCB for the application platform “meltemi” is edge plating (or edge metallizing). Edge plating provides clear measurable advantages at comparably ignorable costs for devices with moderate or high demands regarding EMC, signal-integrity and de-heating. Practice has proved that the theory can be implemented and works.

by Arnold Wiemers

Regarding EMC aspects a device is operating stabile if it doesn’t radiate own interferences (emission) and doesn’t show any reaction to interferences being radiated by other devices (immission). In a technical view these interferences are caused by signal transmission between components of a device or between several parts or boards of a device system. Specific signal transmission in complex multilayer systems takes place via signal tracks on the PCB. Power supply is provided by plane areas or plane layers.

It has to be considered, that for each signal transmission a back current path has to be provided (the so-called GND plane) and that the transport of the information doesn’t take place in two-dimensional packets but three-dimensional electro-magnetic fields. Therefore any device (and any PCB) is a giant electronic microcosm with an hardly imaginable diversity of happenings in smallest spaces.

Herein lies the key for an extended strategy for achieving EMC stability. The construction of a multilayer is done by laying

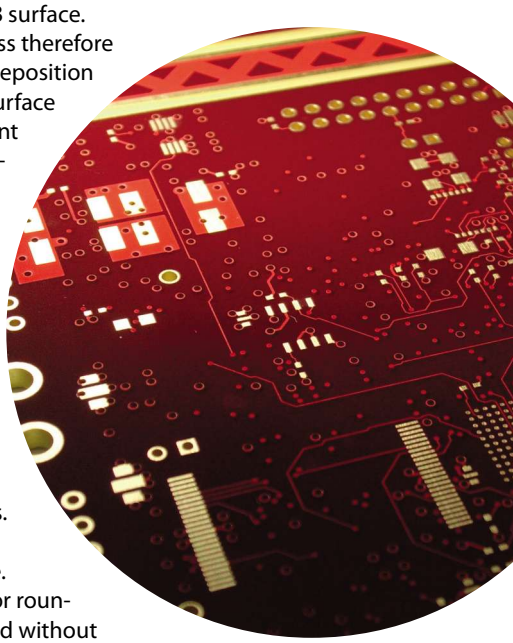
signal layers and power plane layers above each other. During operation of a device created but unnecessary energy is emitted via the edge areas of the power planes. Schematic concepts are trying to compensate these effects, i.e. by termination of signals, by defined signal properties (impedance) or by high-capacitive MultiPowerSystems (MPS). Success of these linear signal transmission can't be comprehensive. An effective control of the electromagnetic fields within the three-dimensional space of the PCB is missing.
However, control can be achieved if field areas are divided into compartments on and within a PCB. In principle the creation of these compartments can be provided via a structured shielding.

EMC behaviour of the PCB significantly improved

Analysing a multilayer construction leads to the simple cognition that each layer is ending rectangular at the PCB edge. In saying so the task is defined: control of the three-dimensional electromagnetic space in a PCB is provided by shielding the edges of the PCB. The prognosis is that in doing so the EMC behaviour of a PCB is significantly improved.

Plating PCB's

In order to give an impression of the function of a shielding it is necessary to describe the electro-plating process. The production step of plating is an elementary one in PCB production. The galvano-technical connection of several layers in a PCB is done by a cathodic-anodic procedure for copper deposition at the inner wall of a drilled hole. In a topological sight the inner wall of a hole is part of the PCB surface.



The electro plating process therefore always causes a metallic deposition on the PCB surface. This surface can be modified in different ways by holes, slots or millings. If the subsequent PCB edge is to be metallised mainly minor logistic re-arrangement of production steps is necessary.
The edge to be plated isn't processed (as usual) in one of the last production steps but has to be carried out already before the plating process. To elaborate the contours milling tools are advisable. With these tools straight or rounded contours are produced without any problem. Cut-outs and/or partial milling of the contour is possible. Milling can be performed to open the contour over the complete thickness of the PCB.

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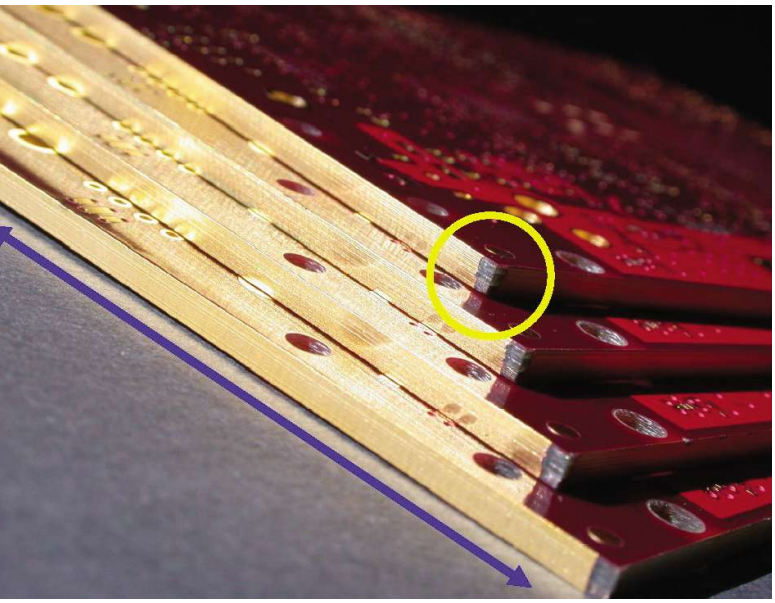


Figure 1:
The edges of all plated contour millings have the same surface plating as the finished PCB

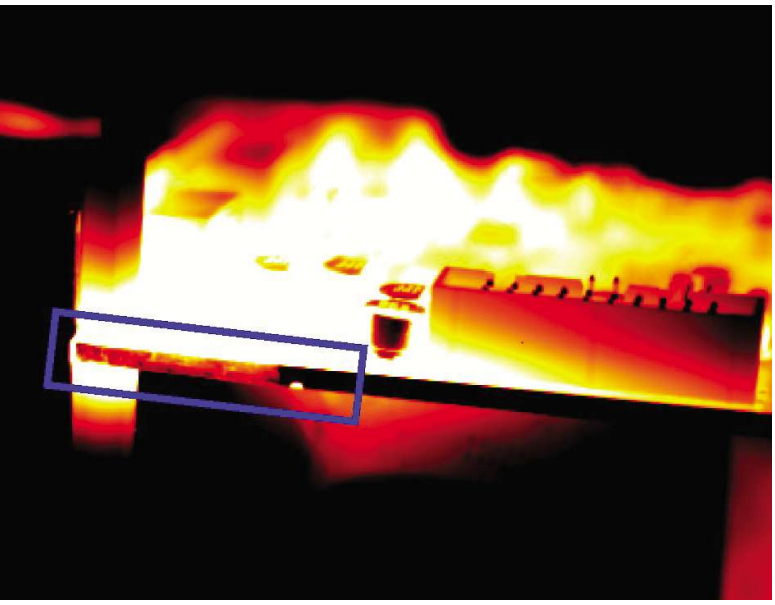


Figure 2:
A compact area on a PCB cannot achieves the same capability for thermal spread and thermal conduction as a metallic band laid around a PCB

Anyhow, it is possible to have plated z-axis millings, opening the panel surface only down to a certain depth. If a plating of the complete outer contour of a PCB is desired it has to be considered that for the following production steps 1-2 mm wide pegs to hold the PCB within the panel are necessary which cannot be plated. The edges of all plated contour millings will have the same galvanic final surface plating as the actual PCB (see figure 1).
Manufacturing costs for plated edges are low. Any manufacturer of PCB's has a galvanic production line and a milling facility. Thus no additional invest in machines or into inventing a new process will be necessary. Only in production process sequences or PPS a decision "edge plating yes/no" has to be invented.

De-heating

Primarily the motivation for edge plating was controlled EMC behaviour. Very soon it was obvious that also the active de-heating of a PCB is improved significantly. Developing of more and more capable and powerful electronics on decreasing space inevitably leads to thermal problems. Conducting the heat by additional measures (heat sinks, casing) is extensive and increases device costs.
One of the strategic aims of CAD design and device construction therefore has to be the integration of de-heating into the multilayer system. In addition to constructive properties of a multilayer (thick copper layers, MPS) the conductive pattern has to be included in the de-heating concept.
The fact that edge plating has more than a trivial share in this purpose arrises from the calculation of the edge surface of a standard euro PCB (100 mm × 160 mm).
The result is a edge surface of $2\,(10 + 16) \cdot 0.15 = 7.80\ cm^2$. In today designs this net area hardly can be kept free on outer layers for de-heating purposes. Additionally the quality of the de-heating via the PCB edge has to be considered. A compact area on an outer layer of a PCB never has the capability for heat spread and heat conduction as a closed area like band laid around the edge of the PCB (figure 2).

Signal-integrity

The component industry already accepted that edge plating in principle is an advantage for signal-integrity in the point of signal transfer from device to periphery. For any demanding electronic system (i.e. LVDS, high speed) the interface from device to cable and/or plug is a vulnerability. For a few millimetres on the way from PCB edge to the cable the shielding or the continuous reliable ground reference for signal transmission is missing. Clearly noticeable disturbances in signal quality can be the consequence. Signal quality can be secured if PCB, plug and cable form an entity.
This task is solved with plugs which are mounted on the plated edge of a PCB. The differential signals are transmitted from the upper and lower region of the plug to the top and the bottom side of the PCB. In the centre area the plug has a metallic joint face that simultaneously provides a reference plane. On the back side this joint face is connected to the partially metallised PCB edge (figure 3). By this means in ideal conditions each signal faces a homogeneous electro-magnetic field from cable via plug to the input component on the PCB.

The result

Edge plating provides clearly measurable advantages at comparable ignorable costs for devices with moderate or high demands regarding EMC, signal-integrity and de-heating. EMC stability of "meltemi" is impressive. And the quote from the EMC test facility "the probe must be damaged, I'm not detecting anything" is already legendary. *(cm)*

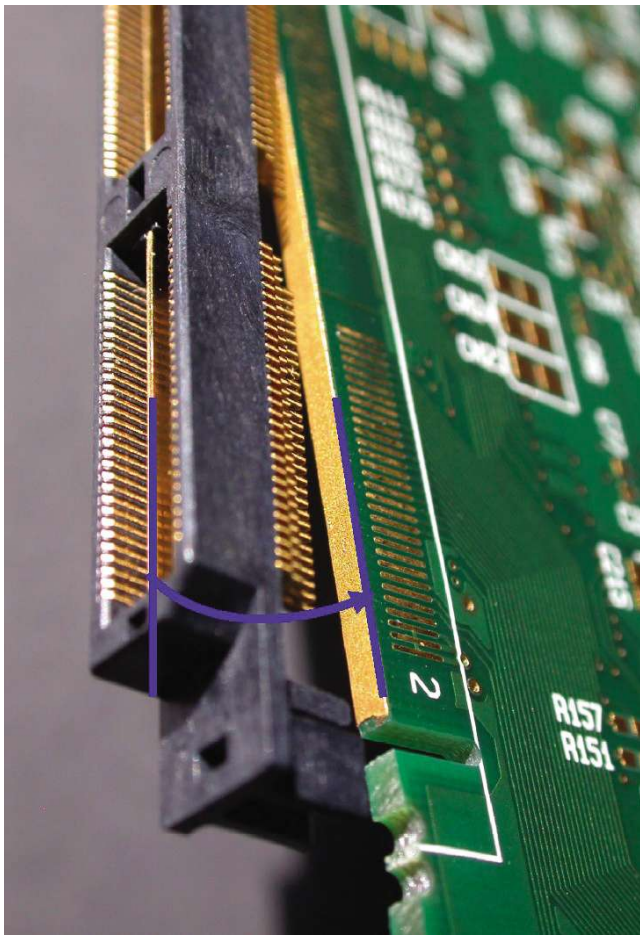


Figure 3:
In the centre area the connector has a metallic joint face which also serves as a reference plane. On the backside this joint face is connected to the partly metallised edge of the PCB.

The third dimension of the PCB

It could be expected that already everything has been thought out. At least anything concerning PCB technology. We left behind HDI and laser vias, next to come is micro fine line technology but that's nothing more than mechanics. Smaller, finer, cheaper are the dicta of PCB technology. Against this background who dares to talk about sensational results for the electro physical properties of PCB's.

Up to now hardly anybody was interested in the edge of PCB

Sometimes solutions are that simple that the question is allowed, why nobody found it earlier. Probably the philosophers among the cryptographers are right in saying "nothing is hidden better than the obvious". Anybody handling PCB's in his all day work knows that there is a component side and a solder side, sometimes called top side or bottom side or primary and secondary side. Are there more layers in a PCB these also are numbered meticulously and certainly get a name.
The third dimension of a PCB, the edge, has no name. Up to now hardly anybody was interested in. This will change in future.





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Chapter 4

Challenges of modern multilayer systems

Elegant Chaos

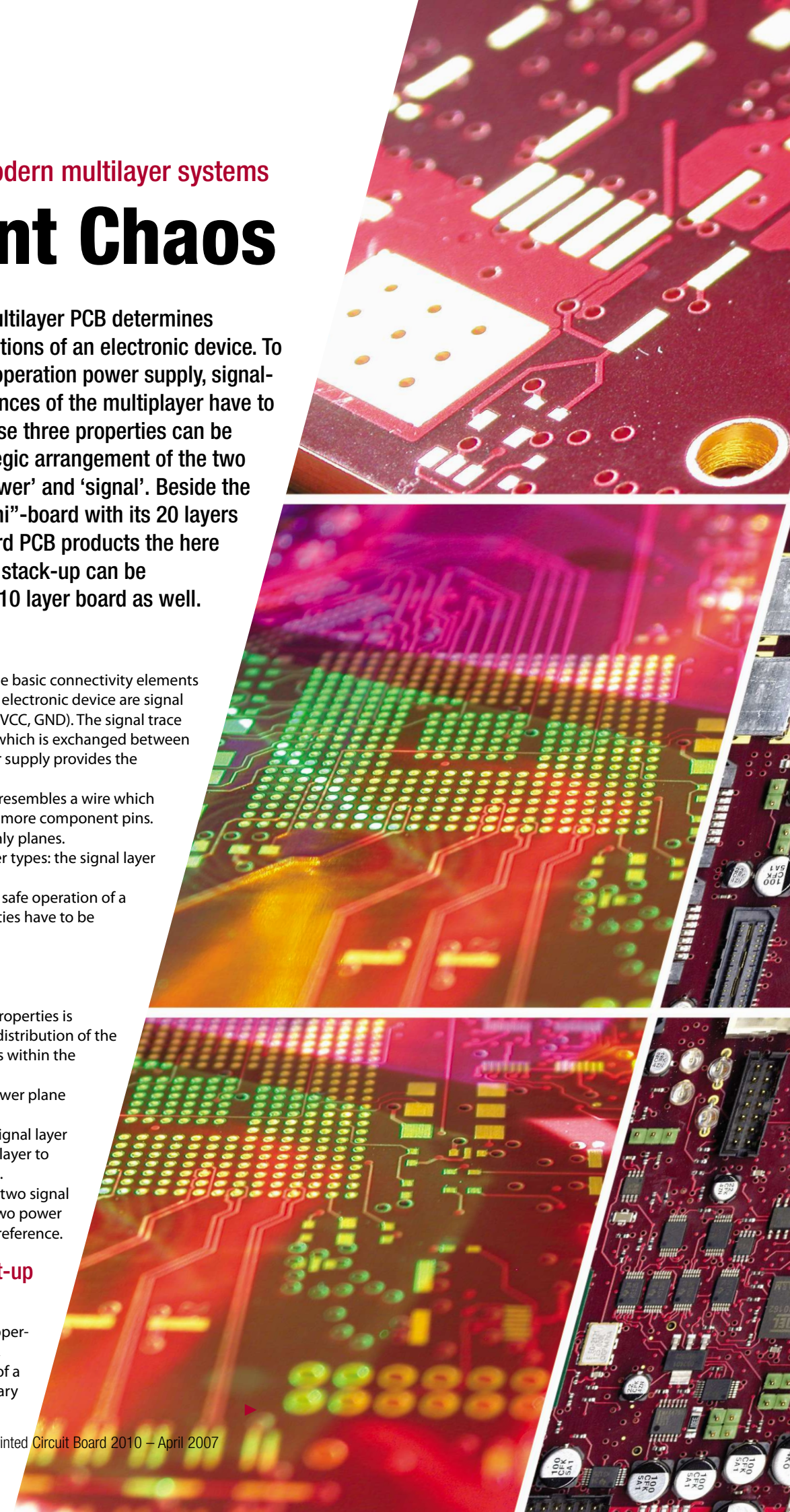
The stack-up of a multilayer PCB determines significantly the functions of an electronic device. To secure the fail-safe operation power supply, signal-integrity and impedances of the multiplayer have to be controlled. All these three properties can be realised with a strategic arrangement of the two basic layer types 'power' and 'signal'. Beside the fact that the "meltemi"-board with its 20 layers is far beyond standard PCB products the here described multilayer stack-up can be transferred to a 8 or 10 layer board as well.

by Arnold Wiemers

Within a multilayer the basic connectivity elements for the function of an electronic device are signal trace and power supply (i.e. VCC, GND). The signal trace transports the information which is exchanged between the components. The power supply provides the required energy.
In principle the signal trace resembles a wire which discretely connects two ore more component pins. Power supplies are commonly planes.
Thus we have two basic layer types: the signal layer and the power (plane) layer.
For the fail and interference safe operation of a device at least three properties have to be controlled:
the power supply,
the signal-integrity and
the impedances.
The control of these three properties is achieved modularly by the distribution of the named two basic layer types within the multilayer board.
Power supply is given by power plane layers.
Signal-integrity assumes a signal layer and requires a power plane layer to secure proper back currents.
Impedance assumes one or two signal layers and requires one or two power plane layers as a capacitive reference.

The geometrical built-up of a multilayer

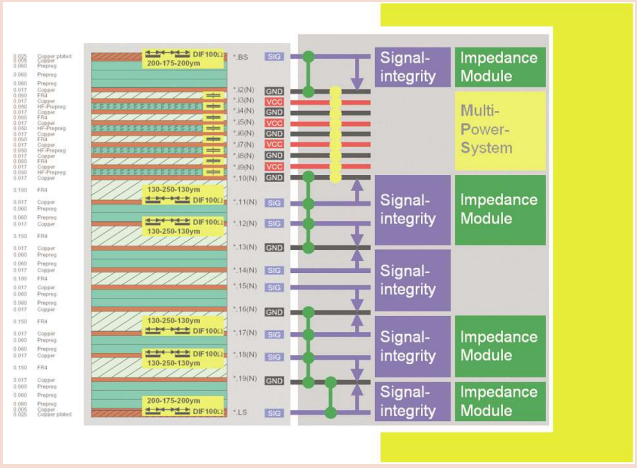
Typical for each of these properties is the fact that only one, only two or only few layers of a multilayer board are necessary



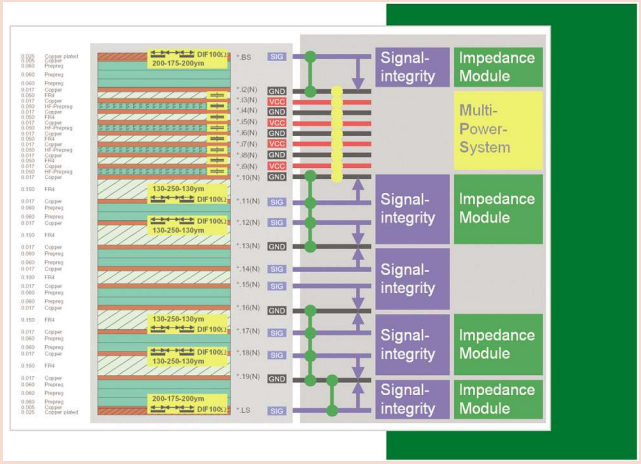
to achieve the functionality. Hence we conclude that these properties are realisable modularly in a compartment of a multilayer PCB.
Consequently we learn that we only need enough layers in a multilayer board to reproduce these modules severalfold. And because only the two elementary layer types signal layer and power plane layer are necessary it is obvious that there must be topological overlaps in the geometrical built-up of a multilayer.

MultiPowerSystems (MPS) – a stapled power supply in multiple adjacent layers

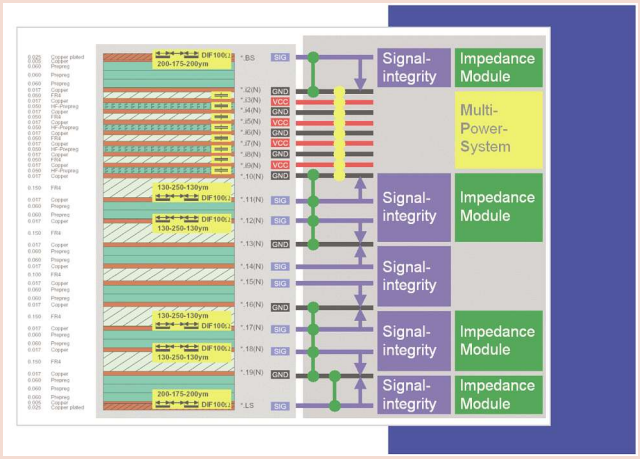
A great advantage for the EMC stability of an electronic device is the possibility of decoupling and buffering of interferences in the power supply. For this purpose the capacity of capacitors is used.However, between power plane layers a capacity exists as well. Sine qua non is that the interacting plane areas are spatial neighboured and that their distance to each other is sufficiently small. Constructing a multilayer system it has be considered that the power plane areas are lying upon each other.
To built up enough capacity the distance between two power plane layers must not exceed 75 µm. Ideally the layer distance is 50 µm. Cores and prepregs of 50 µm thickness are commonly available today.
The capacity of such a power supply system is proportional to its area size. In case that more capacity than available by PCB size is required an attempt is to double the GND plane. If this is still insufficient a complete Vcc plane plus GND plane can be added as a module. Thus a stapled power supply in multiple adjacent layers is built up and we receive a MultiPowerSystem (MPS).
Hereby the global called Vcc planes absolutely can be of different voltages as being usual in practise today.
Important in MultiPowerSystems is that the power supply sequence is top and bottom terminated by a GND plane. Using this construction approach the circuit is shielded against self generated interferences resulting from its own Vcc planes.



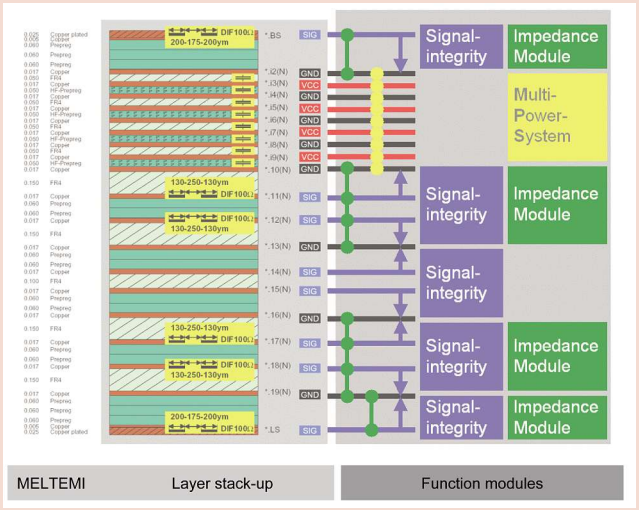
■An advantage for EMC stability of a device is the decoupling and buffering of possible interferences in the power supply



■Considering the impedance of a signal trace provides controlled signal transmission in regard of delay times and trace resistance



■To secure excellent signal-integrity crosstalk between neighbored signal traces has to be minimised as far as possible



■Construction of the multilayer system for the meltemi board

Give modern solutions a chance

Often the approaches to solve a technical task are subject to things in fashion. Anything not being "en-vogue" is overseen or ignored even when physics already doubtlessly decided.
Probably we are living in the electronic era. Definitely we are living in a fraction of time where a solution is preferred instantly when it is consuming power.
The adversities of EMC and signal integrity are combated with electronic solutions. Excessive energies on assemblies are burnt or choked.
It seems to be unthinkable that there might be simple mechanical solutions for many tasks. A fortiori if the dark secrets of interference-free function of a device take place in the interiors of a multilayer board. And even worth if there's no expert team nor a tool. For fashion and elegance of success only one archaic measure exist: independent cogitation.

Impedance of a signal trace

Considering the impedance of a signal trace provides controlled signal transmission in regard of delay times and trace resistance. To realise a certain impedance one or two signal layers and one or two power plane layers are necessary. When routing a signal across several layers within the stack-up the signal must not sustain an impedance change caused by layer change nor should the trace geometry change as far as possible. The impedance value is determined by the trace width on the one hand and the distance between signal layer and power plane layer on the other hand.
Pre-calculated and verified impedance modules can be integrated into the multilayer stack-up. These impedance modules can be subsequently lined-up within the stack-up. Impedance modules which include an outer layer can be applied mirrored to the opposed outer layer.

Signal integrity

The proper back current path of a signal requires a GND plane. To achieve high signal integrity cross talk between neighboured signal traces has to be reduced as far as possible. Furthermore we have to pay attention to the fact that increased layer count commonly impacts decreased layer distances, thus causing in certain cases that the distance between traces on adjacent layers can be smaller than distances on the same layer. Because the information transfer in a signal trace is happening in form of electromagnetic fields high signal integrity is bound to the spatial control of these fields and the controlled back current of the signal via the GND plane.
This requirement is fulfilled when each signal layer faces a GND plane. In order to prevent exorbitant layer count increase a stack-up wherein two signal layers are flanked by two GND planes can be constructed.
Each signal layer takes the respectively nearer GND plane as a reference for it's back currents thus establishing only minor or no interference in the afar distant GND plane.
However from this theoretical conclusion results that maximum two signal layers embedded between two GND planes are possible. Having three or more signal layers in-between would definitely cause cross talk due to overlapping and interacting fields. For signals on external layers only one signal layer above one GND plane is feasible. As a basic principle the use of the external layers if a multilayer as a signal layer is considered as advantageous. Vice versa it is not recommended to use the external layers as GND planes due to combinatory reasons.

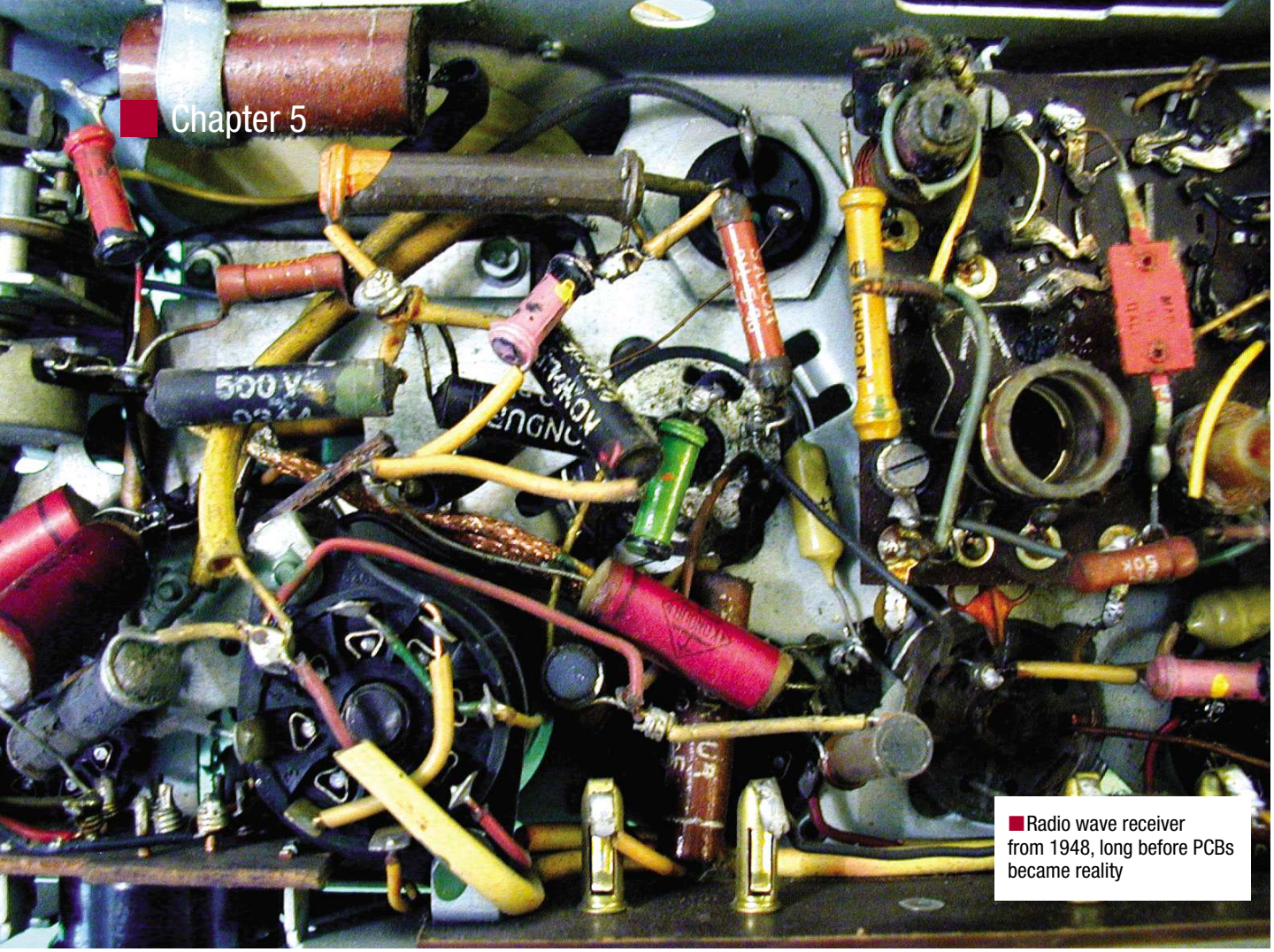
Combination of function modules

The layer count of a multilayer cannot increase arbitrarily nor should it. The analysis of the function modules shows that the requirement for impedance and signal integrity are identical in regard of the mechanical construction principles. Therefore a proper defined impedance module invariably provides high signal integrity. Anyhow the strategic goal in constructing a multilayer-system is always the shared use of power plane layers, especially GND planes. The outer GND planes of a MultiPowerSystem simultaneously form the reference for the impedance and signal integrity modules.

Conclusion

The herein described layer stack-up of the CPU board "meltemi" from unit^el with it's 20 layers certainly isn't a standard product. However "meltemi" shows the combinatory application diversity which by-the-way can be implemented even in 10- or 8-layer boards. Important is that these technical properties are a result of a well-thought multilayer construction.
In fact the physical properties are achieved through strategic layer distribution. The necessity of having to build in two or three more GND planes hereby can be accepted. *(cm)* ■

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Radio wave receiver from 1948, long before PCBs became reality

The Consequences for Layouts and Routing

Just a Piece of Wire

In essence, a PCB trace is nothing but a piece of wire. Such a simple piece of wire has the peculiar characteristic that it both radiates and picks up energy when an alternating current is applied to it. Right from the start, the developers of electronic circuitry have been forced to take these properties of a piece of wire into consideration – whether the goal was to utilize them to form an antenna or to implement measures to reduce undesired emissions to an acceptable minimum in PCB layouts. The controlling elements here are the impedance of a piece of wire or of a trace, as well as the geometry of the circuitry, or the layout and routing of the tracks.

In the early days of electronics – back when tubes were state-of-the-art – people preferred to do the wiring "by hand." Figure 1 shows a radio wave receiver for the long and medium wave band (approx. 300 kHz to 1.5 MHz) in what at the time was already a revolutionary design with a three-dimensional, multi-layer, and multi-level design.
The problems associated with this design were straightforward, and printed circuit boards were still a long way from becoming reality. The focus was on achieving pleasant conditions for working with sinusoidal signals; rectangular signals remained primarily a matter of theory. Any undesired "harmonics" that might arise were simply filtered out. Space was hardly a problem, and EMC was otherwise unknown and, of course, yet unnamed.
Now let us compare that with the "PCB of 2010" shown in figure 2 as an example of a component carrier: There is no steel-

plate chassis; instead it is a multi-layer print with 20 layers; it is manufac-tured using ultramodern technology and populated with highly integrated components.
What do these two modules have in common? Does it even make sense to draw a comparison, or is that just foolishness? Both system designs work without a hitch – including the tube receiver from 1948!
It would even appear that the "wire" in the old tube construction and the wiring on top of and within the multilayer PCB are both governed by the same physical regularities.

What do a radio wave receiver from 1948 and a modern multilayer PCB have in common?

Apparently, the designers of the older device either "instinctively" or consciously (we will examine this question later) did everything right. Most of today's certified "amateur radio operators" are aware of a principle used for antenna technology and wiring technology – a principle that every engineer responsible for routing PCBs and every electronics engineer who designs circuits should even be conscious of in their sleep: The impedance of a wire or printed circuit when an alternating current is applied to it!
There is definitely no way to negotiate with physical realities! We say that as an explicit warning to all those business people who, by hook or by crook, not only want to lower the overall price of a product (as the laws of economics insist they do), but also exert a decisive influence on the technical implementation – without having taken the applicable basic principles of physics to heart.
The unloved PCB is particularly often at the center of attention here: "Two layers really ought to do; one would be even better!" At the very latest, the other side of the coin rears its ugly head in the EMC testing facility. Interestingly enough, the interpretation of the (usually catastrophic) results is then once again the exclusive responsibility of the developer, with the sole exception of the stipulation that the issue must be resolved in a "cost-neutral" fashion.

The peculiar characteristics of a wire or trace in connection with alternating current

While we are on the subject of wire with respect to a trace: How can we, as PCB designers, attempt to visualize this principle? As far as a direct current is concerned, we can imagine a conductive connection between A and B. Through this connection flows a current (I) to which voltage (U) is applied. Given a specific desired current (I), it is possible to clearly determine the maximum acceptable ohmic resistance (R) through the width, thickness, and length of the trace, depending on the trace's ambient temperature. In turn, the maximum required voltage (U) determines the insulation characteristics and the minimum distance between the traces. When alternating current is employed, we must extend this simple "wire perspective" to ▶

Frequency	Depth of penetration
50 Hz	9,38 mm
10 kHz	660 µm
10 MHz	21 µm
1GHz	2 µm

Table: As the frequency increases, the current intensity inside a trace becomes lower than on its surface (skin effect)





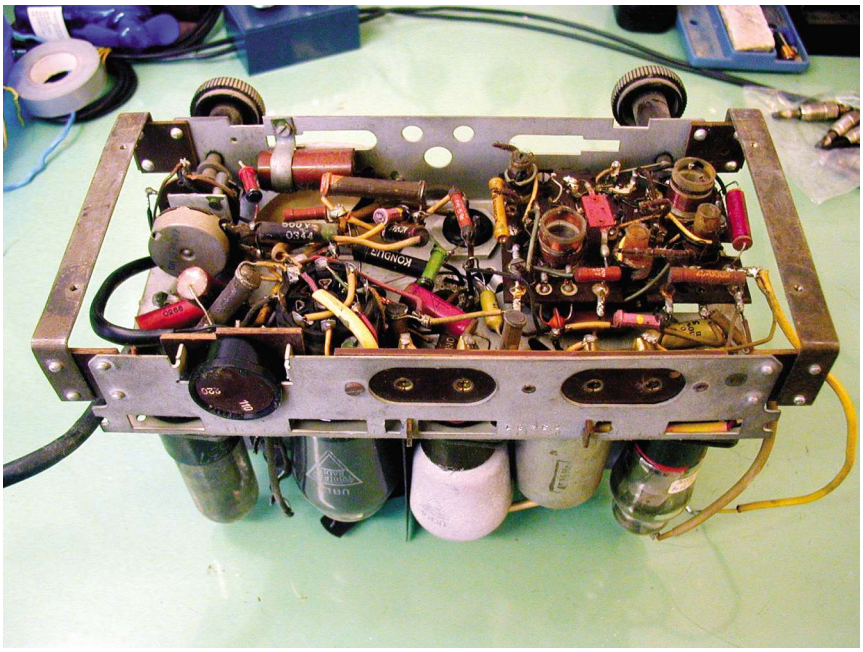


Figure 1:
Radio wave receiver with tube technology wired manually in what at the time was a revolutionary three-dimensional, multi-layer and multi-level technology

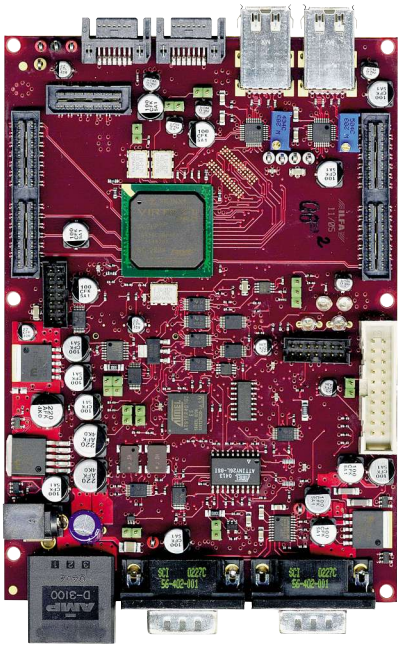


Figure 2:
20-layer "meltemi" board: Module for high speed serial data transmission in the multi-gigabit/s range

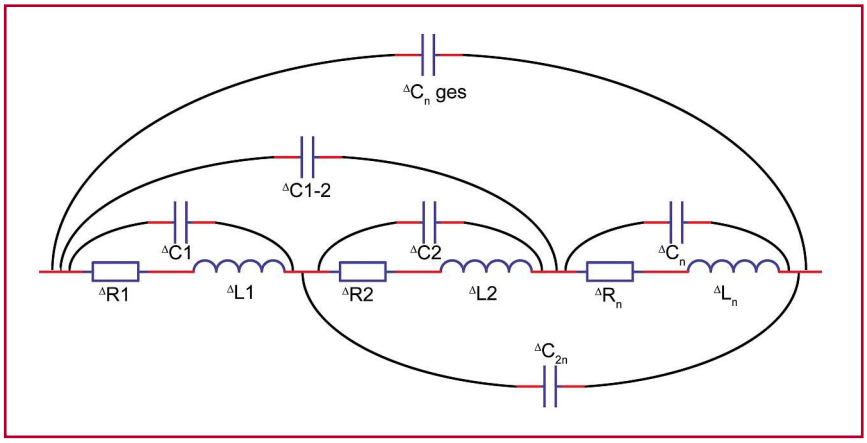
include an additional component that is considerably more complex: The impedance, which stands for a world that is dominated by electromagnetic fields.
As part of their "technical upbringing," RF engineers (and particularly the above mentioned more seldom species of amateur radio operators), learn that a piece of wire of any given length stretched across a vacuum reveals an impedance value of nearly 377 Ω [(120 π) = wave resistance of free space].

A simple piece of wire or trace emits and picks up energy

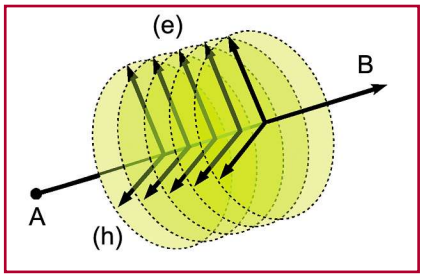
Under the corresponding conditions, the impedance of a dipole line is 240 Ω, and for a piece of wire that is approximately 15 meters long and 10 meters above the ground and with a certain frequency, it is exactly 50 Ω. With other frequencies, it is possible to cover impedance ranges from 140 to 2000 Ω, for example. This confirms our suspicion that the geometry of the wiring apparently has a decisive effect on impedance. This fact is even much more critical for the layout and routing of the PCB.
Unlike the conditions connected with "static" direct current, when dynamic processes are involved, both electric **and** magnetic fields form around this piece of wire or trace. Near the end of the 19th century, Heinrich Hertz, who also established the field of radio engineering with this discovery, recognized a fact that has farreaching consequences: These fields influenced neighboring wires and cables to the effect that part of the "sending wire's" energy was transmitted to neighboring lines that ran in parallel with them. Therefore, we must concede that our simple piece of wire or trace has the peculiar property that it emits energy, and also picks up energy. In other words, we have a sending and receiving principle at work!
From these facts, we can directly derive the following requirements:
a) Do not allow lines to run in parallel for longer distances (avoidance of cross talk).
b) Signal lines **and** their reverse-current lines must be kept as close together as possible.
c) Any change in the geometry of the conductor **or** of the reverse-current line changes the impedance. If we ignore this fact, problems with signal integrity and EMC are unavoidable.

Practical considerations necessitate compromises

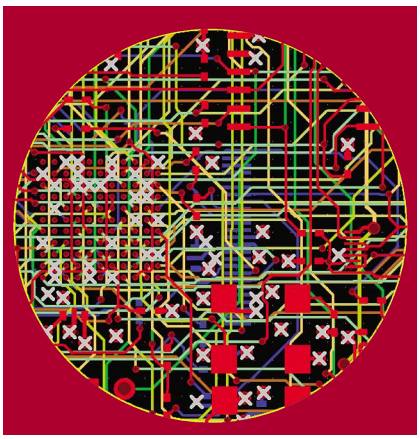
In practice, however, we realize that compromises will be necessary. We can illustrate this with the following example: A via is normally placed at a 90° angle to a trace. For this reason, when perpendicular (orthogonal) routing is used, the wave's polarization results in a more-than-significant factor of 100 for crosstalk (or mutual influence) with the line in its immediate vicinity.
One brief comment on the subject of polarization: Discussions of this topic in technical literature are usually very complicated. For this reasons, it is very difficult to offer a comprehensive definition of this principle.
Basically, polarization refers to the position of an electromagnetic wave's electric field components with reference to a return conductor (usually the earth's surface in antenna technology).
The position of the wave (of the field) is denoted with a direction vector. Using the vectors (graphically), we can add or subtract fields and waves to immediately determine the effectiveness of specific measures designed to suppress fields.
Conclusion:
Just as has always been the case, today's developers and designers are still forced to accommodate the astonishing characteristics that a piece of wire displays when an alternating current is applied to it. This holds true when these characteristics are desired, as is the case when making antennas, and when they are undesired, as is the case when engineers seek to reduce undesired emissions to an acceptable minimum. Furthermore, with the frequencies and switching times employed today, it is becoming increas-ingly the case that we are inclined to "forget" to take the depth of penetration (skin effect) into considera-



■ Figure 3:
Equivalent circuit diagram of a conductor: In a vacuum, a piece of wire of any length has an impedance of nearly 377 Ω [(120 · π) = wave resistance of the vacuum]



◀ Figure 4:
Propagation of a wave: A – location of the emission, AB – direction of propagation, e = electric field, h = magnetic field



■ Figure 5:
Example of trace routing: None of the structures run in parallel on the meltemi board; comparable with the manually wired "multi-dimensional" construction in figure 1

tion. As the frequency rises, the current density inside the piece of wire or trace becomes lower than on the surface (see table).
For PCBs (material Cu, εr = 4,3), the following rule of thumb can be viewed as sufficiently accurate: skin depth in Cu/mm = 66.3/(√(f[Hz]))
Ultimately, only the results matter: Whether they have been "distilled" from empirical experience, calculated through laborious mathematical processes, or purchased using expensive software packages. *(cm)*

References:
Fig. 1: Alfred Obermayer (OE3AOW), amateur radio operator, radio receiver pictures;
"Rothammels Antennenbuch"
Frank Sichla (DL7VS), "Die HB9CV Antenna";
Pierre Villemagne, "Antennen für die unteren Bänder"
Hannu Tikkanen, "Printed Circuit Board Design Guide"
"ARRL Handbook 2005" (American Radio Relay League)
Heiko Dudek, Cadence Designs Systems: "Differenzielle Signalführung in PCBs" ■

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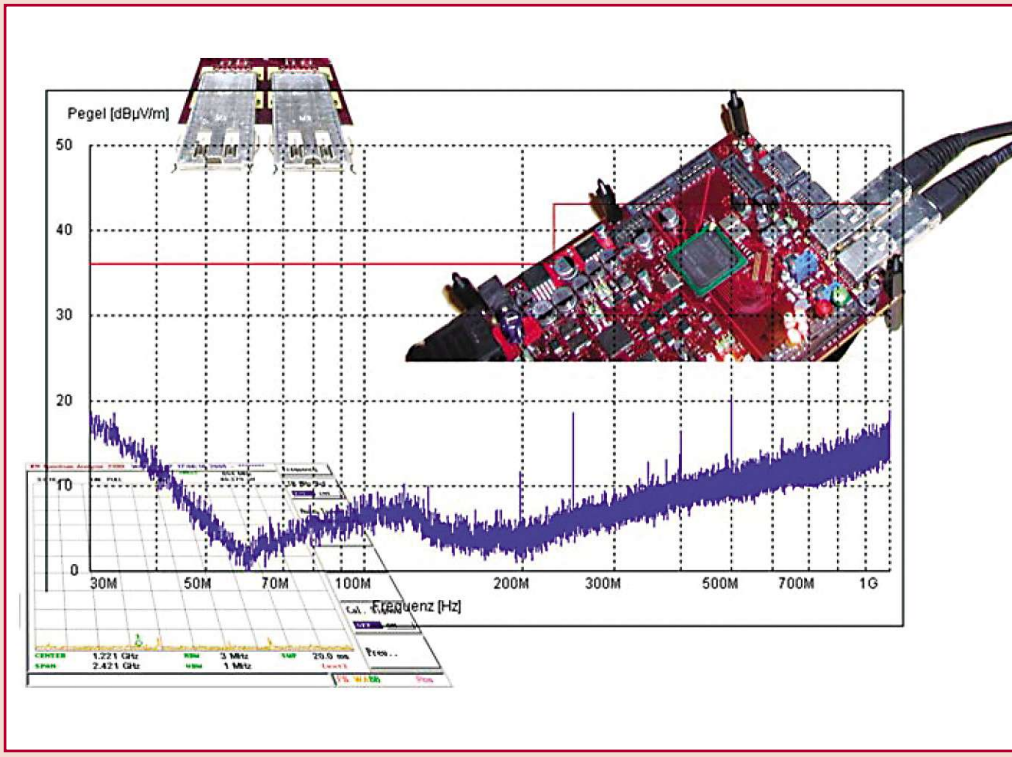
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Analysing signal quality of transmission lines

In the EMC Test Facility I

Signal-integrity encloses all problems which occur in line connections within hardware for high speed applications. FPGA's with their multiple programmable I/O-blocks are ideally qualified for analysis of the signal quality of transmission lines on PCB's and their connections to connector components. In this chapter we examine the signal quality of data transmission lines between SDRAM and FPGA of the 20-layer "meltemi" board referring to measurement results.

by Gerhard Eigelsreiter



Integrity: a synonym for the continuous consensus between ideal and reality, in practise arising values, not in every detail but en bloc. A paraphrase which in regard of signal-integrity allows a well and truly degree of free interpretation.

In electronic signal-integrity commonly implicates all problems occurring with high-speed applications in hardware devices.

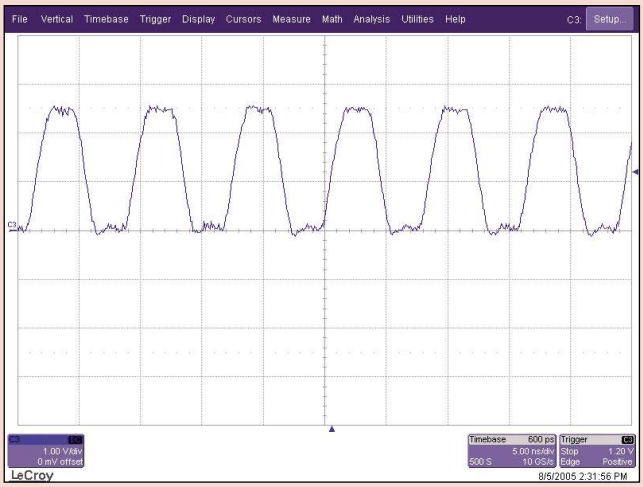
Regarding transmission rates of 1 Gbit/s and more it has become rather popular to launch hardware products which barely hit the road in the EMC test hall. Thus inevitably functional stability goes to the dogs which in the innocuous cases is reflected clearly in significant decrease of the actual transmitted user data. Thereby the bandwidth in the I/O domain presents itself increasingly as the central requirement for flexible core hardware with long life cycle in market segments with rapid changing product cycles and product adaptions.

Implementing increasingly intricate circuitry tricks and resource guzzling mathematical algorithms failure recognizing and correction procedures are fine tuned until paper is packed over all deficiencies at cost of transmission rate that the majority of users is not right at the end of their tether but just slightly disgruntled as being used to since ever. Indeed the so found solution could be used much more efficiently for exploitation of existing channel capacities, provided functional stabile and EMC compliant constructed hardware. Finally only on stabile hardware low-error respectively error-tolerant software can be realised in long-term economic perspectives. Therefore it is necessary to constructively counteract the in many electronic fields increasing interfering emissions.

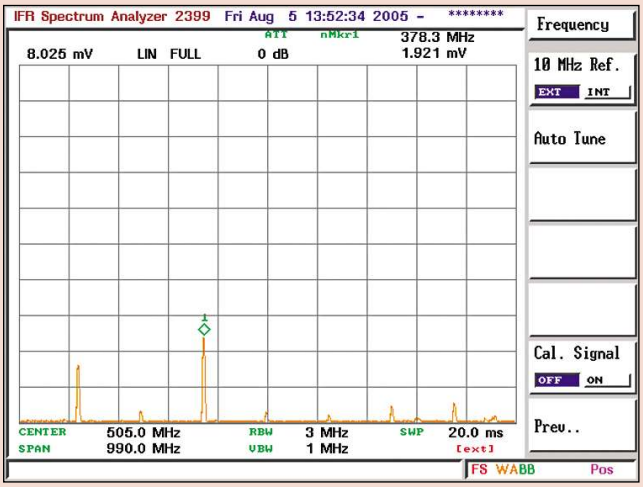
Checking signal-integrity of data transmission lines

FPGA's with their manifold programmable I/O blocks are ideally dedicated for analysis of signal quality of transmission lines (i.e. signal traces on PCB's) and their interconnection to connectors which exist already as fixed hardware and often as final board solutions. Based on measurement results the signal-integrity of data transmission lines between SDRAM and FPGA of the 20-layer "meltemi" board shall be examined and demonstrated. For this purpose the data signal line "DQ26" (overall length 17 mm with an added via for layer change after 11 mm) and the data signal line "DQ23" (overall length 53 mm but without layer change and therefore without vias) are examined. Both signal lines are impedance defined with 50 W and routed accordingly.

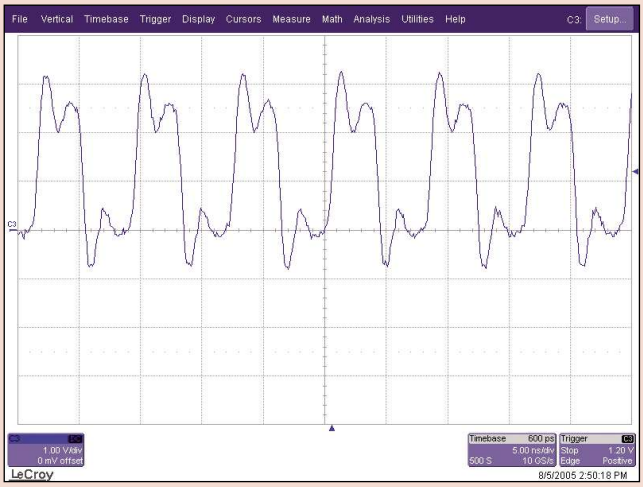
Figure 1 and 2 show a 125 MHz signal on "DQ26" signal line at a driver adjustment of the FPGA I/O block in the "12 mA Slow" mode. This approximately matches a driver output impedance of 50 Ω. Expectedly the oscilloscope displayed a proper signal. The same line in the "24 mA Fast" mode is displayed in figure (resembling approximately 20 Ω driver output impedance). Regarding EMC more than critical. Refer to figure 4 (measurement with h-field probe and ▶



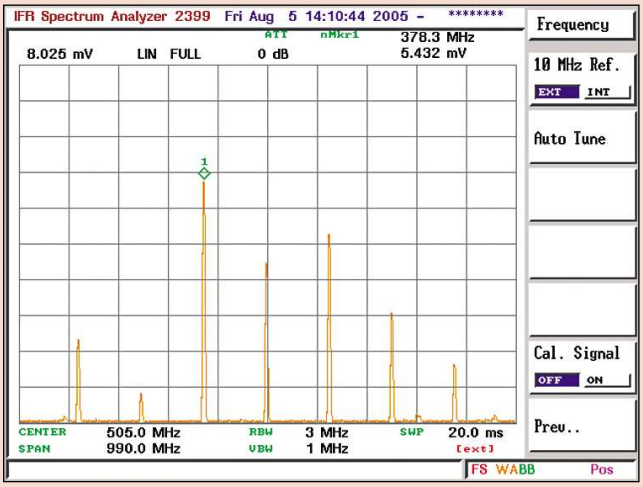
■ Figure 1:
The FPGA data signal “DQ26” in “12 mA Slow” mode, 125 MHz
Good signal quality



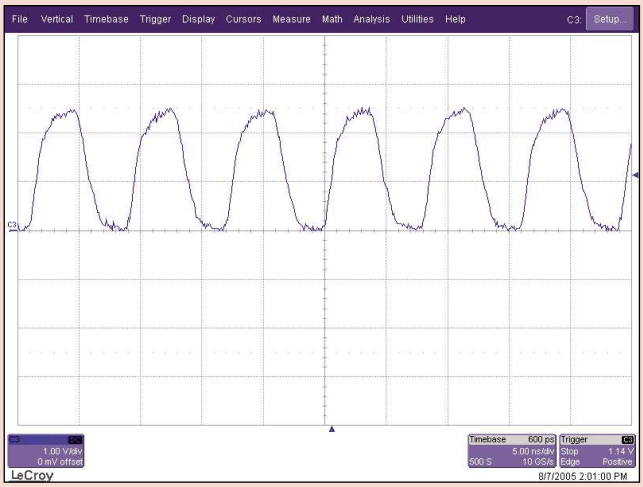
■ Figure 2:
H-field probe measurement of “DQ26” at the SDRAM input pin,
“12 mA Slow” mode



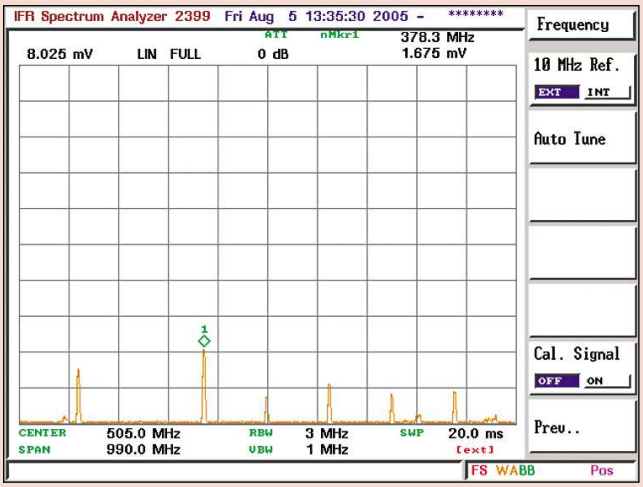
■ Figure 3:
The FPGA data signal “DQ26” in “24 mA Fast” mode,
Signal quality in a critical range



■ Figure 4:
H-field probe measurement of “DQ26” at the SDRAM input pin,
“24 mA Fast” mode

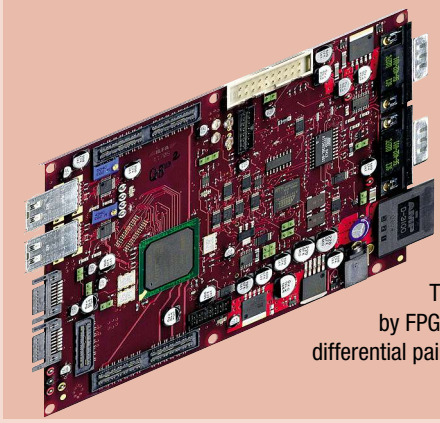


■ Figure 5:
The FPGA data signal “DQ26” in “DCI” mode, 125 MHz
Good signal quality



■ Figure 6:
H-field probe measurement of “DQ26” at the SDRAM input pin,
“DCI” mode (so called “automatic”)

The high speed platform meltemi – hardware with long lifecycle



Lynchpin of the "meltemi" board is a FPGA with integrated serial transceivers surrounded by fixed connected supporting logic and a 32-Bit single chip microcontroller. The I/O-ports lead out by FPGA are routed with differential pairs. 61 of the 77 differential channels are laid out in LVDS technology with transmission rates of 600 Mbit/s per channel meaning altogether more than 36 GBit/s gross.
The remaining 16 channels are covered by 8 integrated transceivers with 2.5 GBit/s per channel, altogether 40 Gbit/s gross. Four transceiver connections run across each to infiniband and two serial ATA connectors towards periphery. The remaining four transceivers as well as the 61 LVDS pairs are using four impedance defined high-speed socket connectors to provide piggy-pack capabilities. The two infiniband-connectors are not directly interconnected with the transceivers: data transmission via cable connection up to 17 m are secured by adaptive cable drivers and -equalizers.

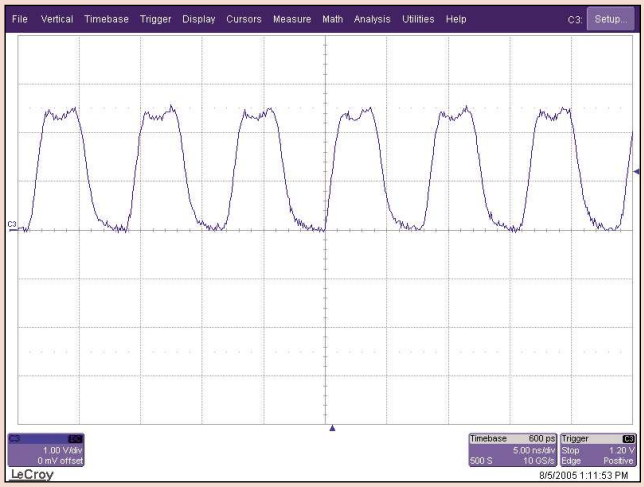


Figure 7:
The FPGA data signal "DQ23" in "DCI" mode, 125 MHz
Good signal quality

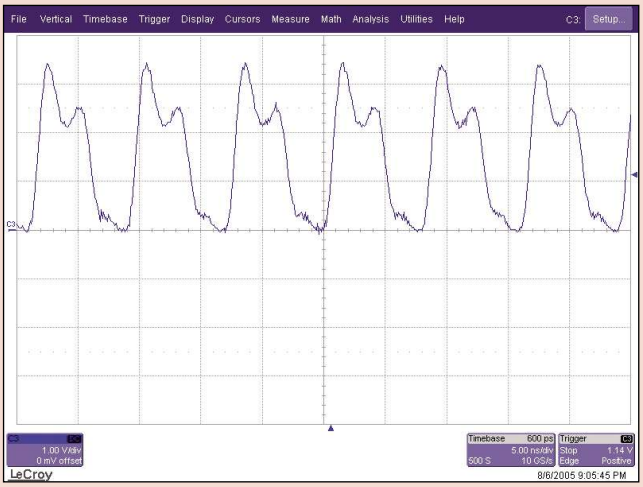


Figure 8:
The FPGA data signal "DQ26" in "DCI" mode ("automatic"), 125 MHz
Signal quality in a critical range – The only difference to figure 7: the measurement has been made on a different day!

spectrum analyser. The results obtained in the EMC-test facility confirm the first impression.
The driver adjustment can as well be chosen in a kind of automatic mode (DCI mode) which continuously readjusts the driver output impedance in reference to temperature and voltage fluctuations using a 49.9 Ω reference resistor (figure 5 and 6). This elegant solution found favour with the next measurements on the signal "DQ23" (figure 7). Repeating the measurements under same measurement conditions on the next day caused big surprise (figure 8). The day after during the third measurement session caused deep suspiciousness receiving identical results as in figure 7. Even with the broadest view such differences can't be simply declared with errors of measurement especially seeming to be day dependent.
A circumstance that definitely couldn't be accepted. The answer to this problem having major future impact for EMC purposes and thus causing functional instabilities is to be read in the next chapter. *(cm)*

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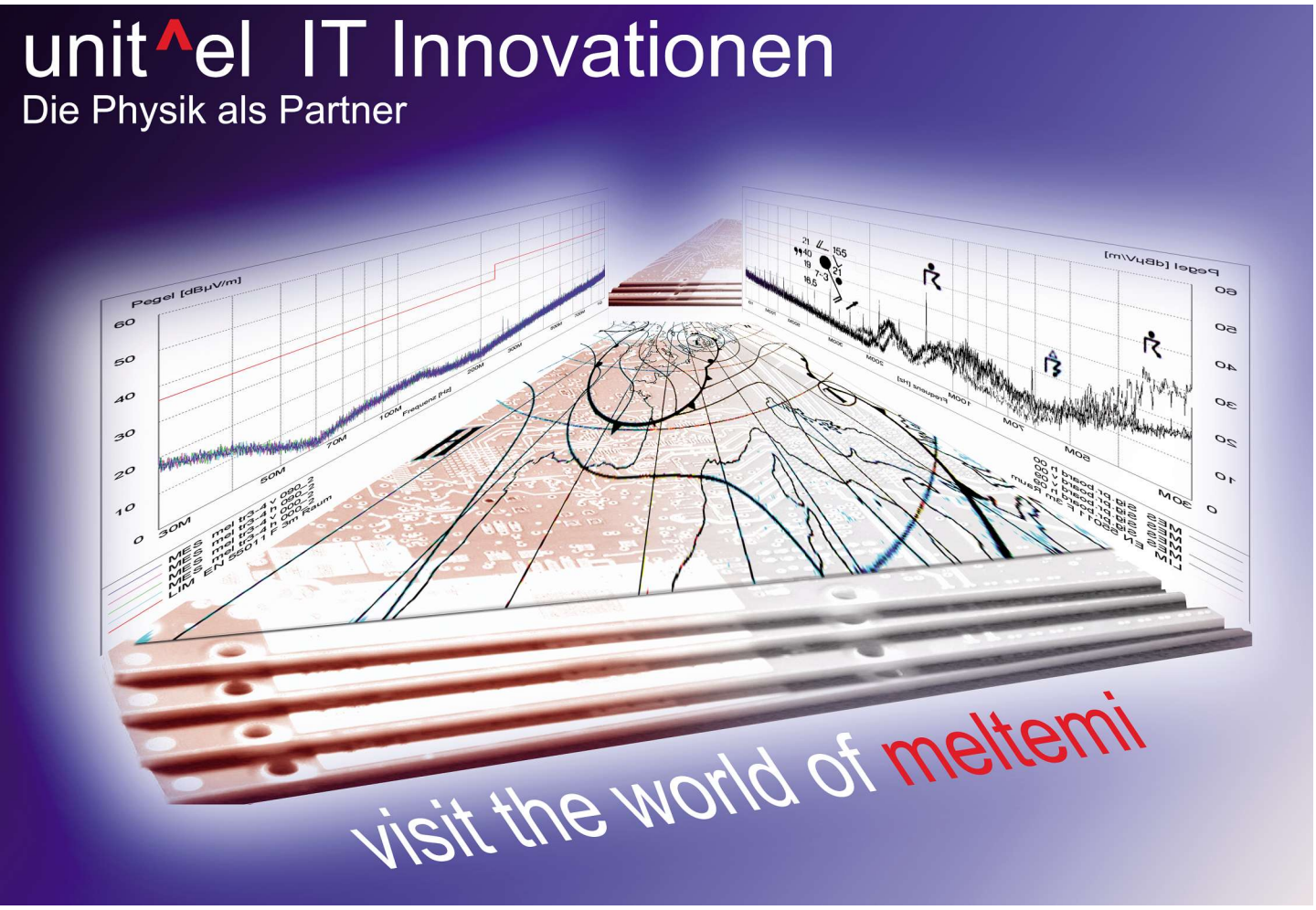
The influence of programmable logic on EMC emissions of a device

In the EMC Test Facility II

The in chapter 6 described seemingly day dependent signal-integrity measurement results in spite of identical measurement set-up and identical IOB settings of the FPGA triggered intense research activities in the development team of the high-speed application platform "meltemi". During the fault analysis a fine but significant difference became clear: the installed FPGA software was responsible for passing or not-passing the EMC test.

by Gerhard Eigelsreiter

According to a legend the term "bug" was found in the early times of computers when insects influenced the function of relays in big machines and even caused short circuits. For noise and crackle in telephone lines small animals had been made responsible as well, being rumoured they were continuously nibbling the cables.
A malfunction due to a moth in the relay circuitry of the computer "Mark II Aiken Relay Calculator" in the 1945 is told to have led to the statement of computer pioneer Grace Hopper "First actual case of bug being found". Moth and log page nowadays are to be found at the Smithsonian Institute. As it behoves for insects these bugs proliferated rapidly and preferably appear in huge swarms.



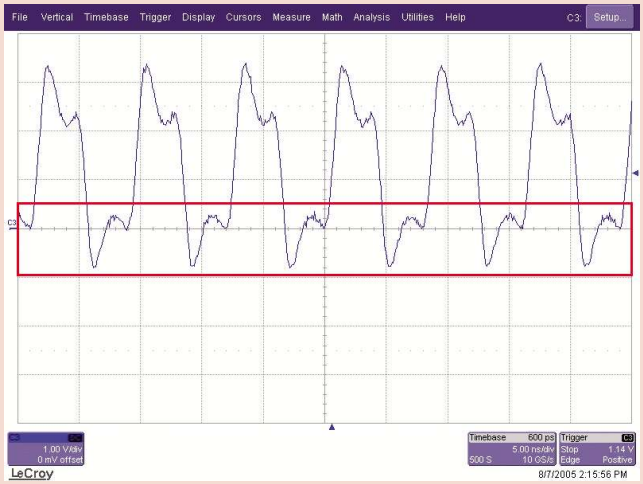


Figure 1:
The FPGA data signal line "DQ23" in "24 mA Fast" mode 125 MHz; lower signal half (red mark) – signal quality in critical range

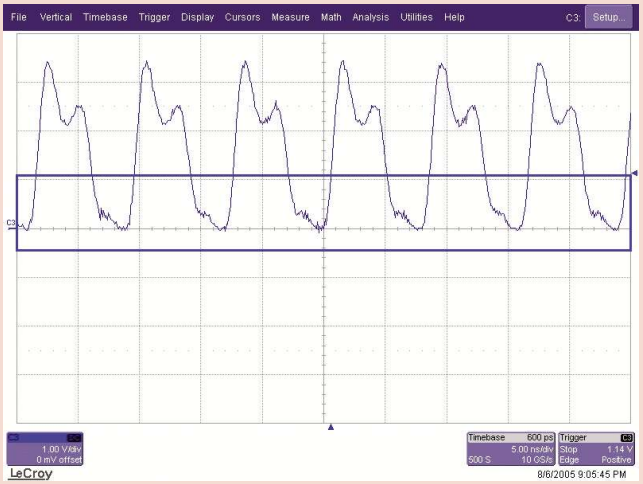


Figure 2:
FPGA data signal line "DQ23" in "DCI" ("automatic") mode 125 MHz; upper signal half – signal quality in critical range; lower signal half (blue) – good signal quality

The "insect" control of these therefore takes place area wide with so-called "service Paks".
Meanwhile the bugs spread out in direction of signal-integrity and EMC preferably using re-programmable logic.

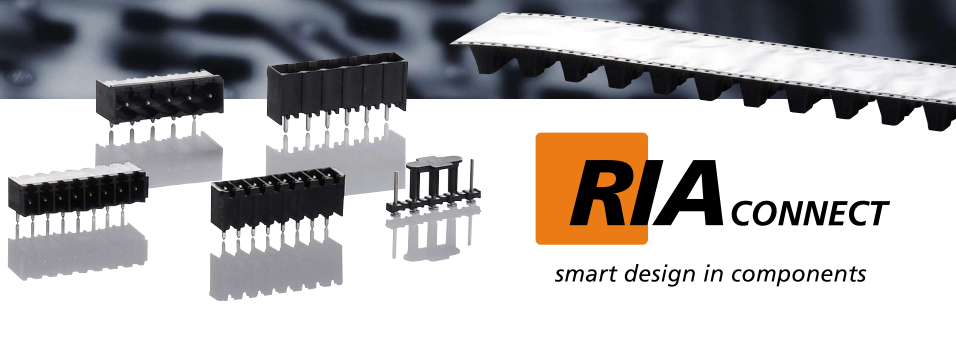
Reasons for day dependent results in EMC test

Day dependent results as described in the chapter "signal-integrity I" in chapter 6 nearly automatically trigger intense research activities when found in signal-integrity measurements. The direct comparison of the measurements on the data signal line "DQ23" (input pin of the SDRAM) in "24 mA Fast" mode (refer to figure 1) to "DCI" ("automatic") mode (refer to figure 2) show in the upper half's of the diagram (blue and red marks) amazing correspondency. A higher resolution of the measurement in the time scale clarifies the problem.
Comparing the rising slope of the graph of both measurements at the low/high switch hardly a difference in rise times is recognisable. All the more remarkable that this is contributed to the fact that it is the shortest rise time possible by software indirectly adjusting the driver current. On the other hand the falling flanks, meaning the switch from high to low, show significant differences.
The rise time (blue mark) of the signal in "DCI" ("automatic") mode in figure 4 nearly exactly represents the "24 mA Fast" mode while the fall time (red mark) equals the desired "DCI" mode in correct mode of operation. How can this occur?

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Is it possible to program rise and fall times seperatly. Is doing so useful at all? Naturally not! Being the answer to both of the last two questions.
The explanation, how this can happen at all is only suspicious. In spite of identical measuring setup and identical IOB settings of the FPGA a slight but finally decisive difference was found. The schematic for this test scenario was designed with logic symbols which in fact already represented the graphical appearance of the included VHDL code. The translation of the VHDL code until the generation of the desired load bit current sometimes took up to ten minutes (naturally being strongly dependent from the performance of the used PC).

Different results due to software bugs of the FPGA's

As hundreds of measurement sequences were waiting to be carried out a software shortcut in form of the FPGA editor module was used. Gain of efforts was a cut down of elapsed time for bit current generation below two minutes, and coinstantaneous the solution to this phenomenon. Using the FPGA editor allows to set the attributes in the IOB's, comparable to a hex editor of a software.
After a two day research the differences in the graphs could be created reproducible. Each time when the translation by the VHDL compiler as well as the appropriate map-and-place software generated the load bit current the undesired differences in the rise and fall times occurred. Each time the FPGA editor was used the result was correct and the rise and fall times were moderate according to the defaults of "DCI" mode.
Well, probably one more software bug?! Shrug your shoulders, who cares, let's get the next service pak! Really nothing more than an unimportant trouble? A glimpse into the EMC test facility is teaching us better. In order to give a clearly arranged overview in the graph 16 data signal lines ("DQ16" to "DQ31") were driven in parallel with 100 MHz and examined in the EMC test facility. Figure 6 represents the 16 data lines in correctly working "DCI" mode.



Figure 3:
FPGA data signal line "DQ23" in "24 mA Fast" mode in 1/ns division, meaning higher resolution. The rise time (blue) and the fall time (red) nearly are identical.



Figure 4:
FPGA data signal line "DQ23" in "DCI" ("automatic") mode in 1/ns division, as well higher resolution. The rise time (blue) and the fall time (red) are significantly different.

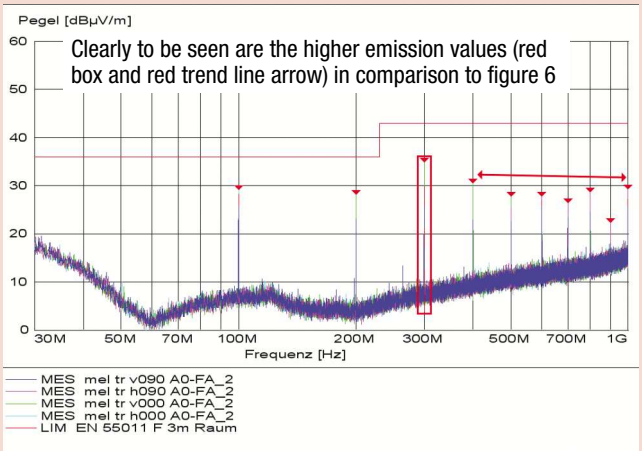


Figure 5:
Interference spectrum of the "meltemi" device from the EMC test facility: 16 data lines ("DQ16" to "DQ31"), "24 mA Fast" mode

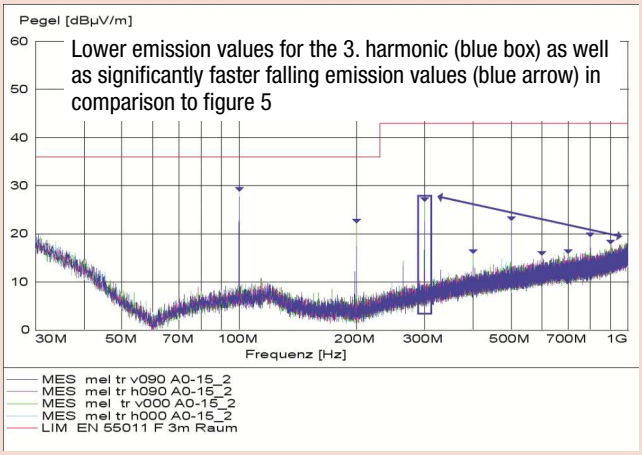


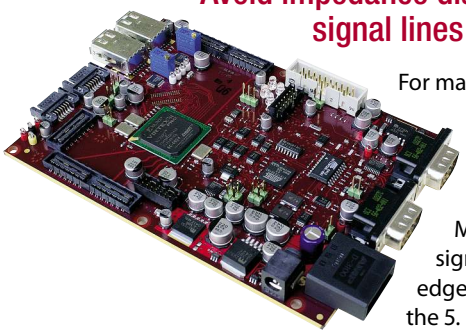
Figure 6: Interference spectrum from the EMC test facility: 16 data lines ("DQ16" to "DQ31"), in "DCI" ("automatic") mode in correct operation mode

The perfidies of FPGAs

Manufacturers of measurement equipment are facing a golden age. Setting aside an appropriate signal quality measurement before the EMC test easily can lead to exceeding the limit values in an extent that doesn't allow a positive judgement of the EMC test results anymore. Abandoning re-programmable logic in future surely can't be sapience's final conclusion because an increasing number of semiconductor producers is planning to equip micro controllers with integrated re-programmable logic. Meaning we can only hope for a short period of grace, not more. Hoping that software update will fix the problem on the other hand could work out being deceiving.
Being safe is only possible by direct measurements. Finally the functional stability of the entire device probably will suffer from the possibility of dynamical reload (hardware update) of i.e. FPGA based hardware via internet or company based client networks – with consequences that potentially aren't foreseeable.

Figure 5 represents the interference spectrum in "24 mA Fast" mode. The differences manifesting in up to 7 dBµV/m higher emission values especially in the higher harmonic vibrations like the 3. harmonic (refer to blue mark in figure 6 and red mark in figure 5) as well as the 5. and 7. harmonic (refer to blue mark in figure 6 and red trend line arrow in figure 5) are clearly recognizable.
While the basic frequency of 100 MHz representing the 1. harmonic shows nearly identical values – and naturally has to. It doesn't sound much, however it's only 16 data lines.
In practice a significantly higher number of lines for data-, address- and control signals has to be considered. Higher emission values – so to be spoken – are program.

Avoid impedance discontinuities on signal lines as far as possible



For many micro processors and ASIC's the bandwidth can be estimated by the thumb rule BW(clock) = 5 · f(clock). Meaning an even more significantly contribution to edge steepness is caused by the 5. harmonic.
At a 100 MHz clock rate a 500 MHz bandwidth can be estimated. However, the rule of thumb only works having good signal quality provided.
In case of ringing and reflexions (figure 1) significantly higher frequency parts, meaning beside all un-equal harmonic vibrations all equal harmonic vibrations as well, have to be taken into consideration. This being a major reason why alone from clock frequency no usable evaluation for expected emission values can be estimated.
Therefore it is that important to avoid impedance discontinuities on signal lines as far as possible or at least keep them as small as possible in number. Plane power supply systems (Vcc and GND plane layers) necessarily have to be included into these considerations (refer to link "publications from Prof. Christian Dirks", see page 80). *(cm)* ■



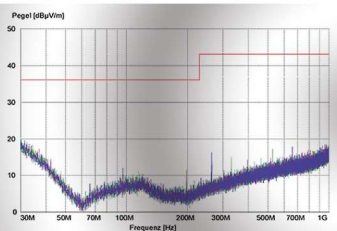


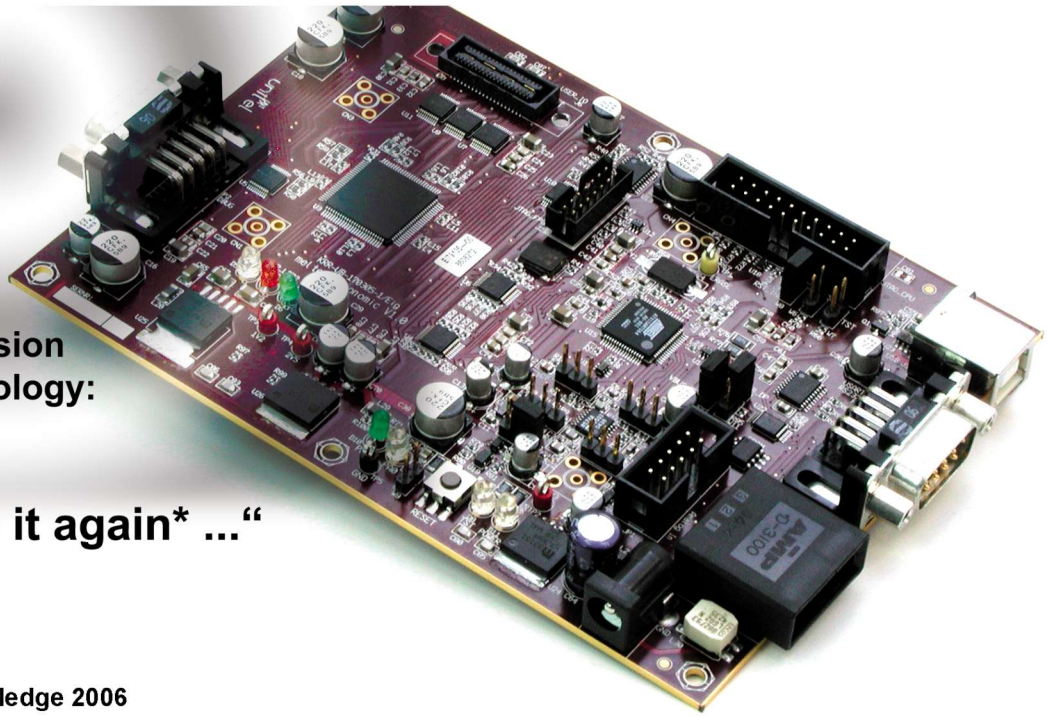






meltemi economic





"Downward progression of the metemi-technology: 6-layer board!

we will never do it again* ..."

***this being our New Year's pledge 2006**

Squaring the circle I

Stable Hardware in 6 Layers

The "meltemi" platform is designed for applications for image processing, HDTV or digital TV, where loads of data are to be transmitted. Transmission bandwidth of up to 60 Gbit/s associated with excellent EMC behaviour and maximum functional stability and reliability are achieved through a 20-layer board with integrated MultiPowerSystem, impedance defined trace routing, X2Y capacitors and edge plating.
In this and two following episodes of our series you will learn if and how the experiences made in constructing 18- and 20-layer boards regarding EMC and functional stability can be transferred or better compressed approximately loss-free into a 6-layer-board design with single sided assembly.

by Gerhard Eigelsreiter

The term "economic" implies fairly presented, cost-effective, profitable and efficient, all together known as the economic principles. Efficiency commonly is described as the relation between a benefit, which naturally has to be given in a defined quality, and a certain effort which has to be made to achieve exactly this benefit. If the wherewithal can be kept as small as possible for this purpose by efficient behaviour one of the clues of the economic principles has been found. Unfortunately blind trust or overconfidence in the optimum principle, meaning achieving a maximum yield with minimum wherewithal leads to unplanned activities, because usually no clear requirements are defined and no clear aim is given. Such course of action isn't effective at all. To achieve preset objectives sustainable activities have to be implemented step by step with constant mutual verification.

Compress experiences made with 20-layer-boards

Theory and it's all very well to say that but what is practise like? Is it possible to compress experiences made with 18-layer and 20-layer-boards regarding EMC and stabile functionalities nearly loss-free into a 6-layer-board design?

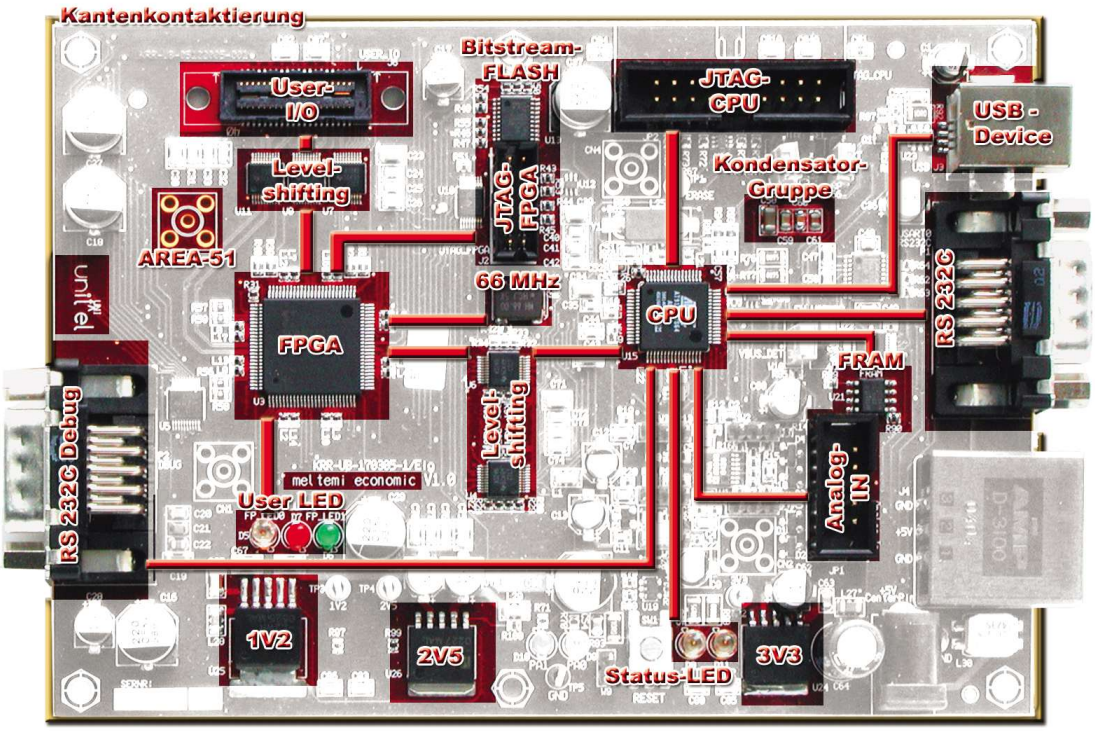


Figure 1:
Block diagram of the "meltemi economic" device: 32-bit microcontroller and flexible I/O-structure; free programmable hardware accelerator or re-programmable logic tops off the range of application and extends the life cycle of the hardware.

Taking unlimited masochistic attitudes into consideration the answer is: Clearly yes!
A narrow view into the catalogue of necessary technical measures doesn't show major obstructions. This remains true as long as the glimpse on it is respectively short.
But the devil is in the details. A descriptive explanation can be given on the basis of the reference platform "meltemi economic".

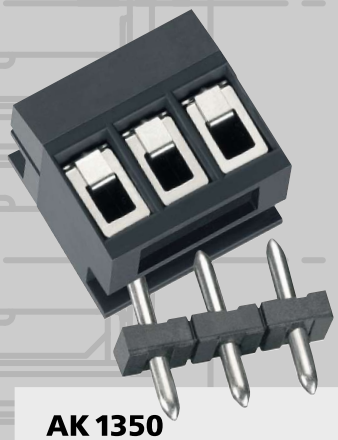
Defining the layer number and choosing the components

After having developed the entire technical concept of the meltemi economic board taking especially the economical aspects into consideration (the costs for the hardware should be low or better "nothing") the next step before drafting the schematics is defining the layer number and stack-up as well as choosing the necessary components. Both are that important because the manufacturers of semiconductors in their restless efforts to force innovation equip the active components with manifold additional supply and operational voltages.
The predefined maximum layer number of 6 layers with a special allowance of broadband decoupling power supplies by the general concept therefore significantly restricts the component choice. Additionally the enormous cost pressure leads to a special predicate "running the gauntlet with interesting, because unexpected and unknown side effects" for this kind of development.
Now the details: A useful reference hardware should cover the microcontroller domain with a single-chip-concept – optimal were 32 bit internally – as well as additionally a highly flexible I/O-structure due to signal-integrity aspects. Free programmable hardware accelerators or re-programmable logic round off the range of application. They shall especially provide a substantial extend of the life cycle of the hardware and contribute to easier fulfilment of economic aspects.

The target: Hardware with long lifecycle

Based on cost reasons and market penetration the 32-bit embedded processors of the ARM7-series were chosen. The long lasting market leadership in the 32-bit-microcontroller field and the comprehensive software pool mainly led to this decision. Taking the semiconductor producer Atmel and the AT91SAM7S family is based on the comprehensive roadmap as well as the technically very flexible, pin-compatible members of this micro-controller family.
More than 20 years of experience with re-programmable logic from Xilinx nearly inevitably forced us to chose and employ the Spartan-3-FPGA-family to secure a maximum of I/O-flexibility.

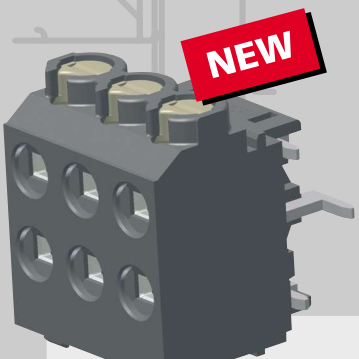
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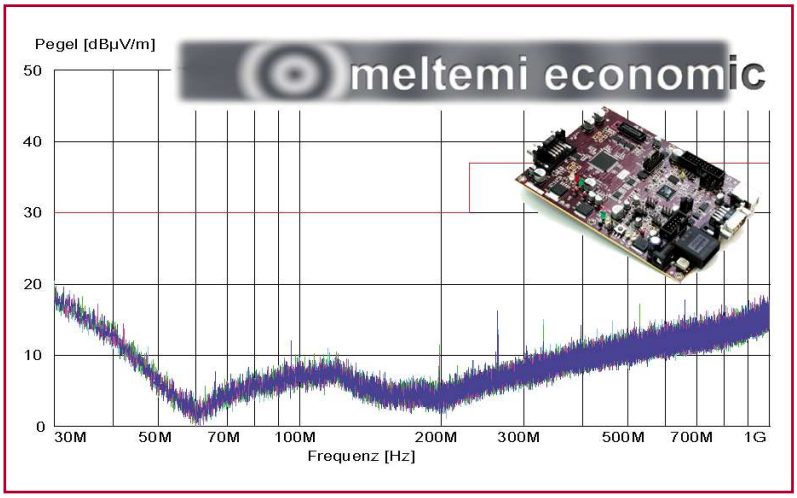
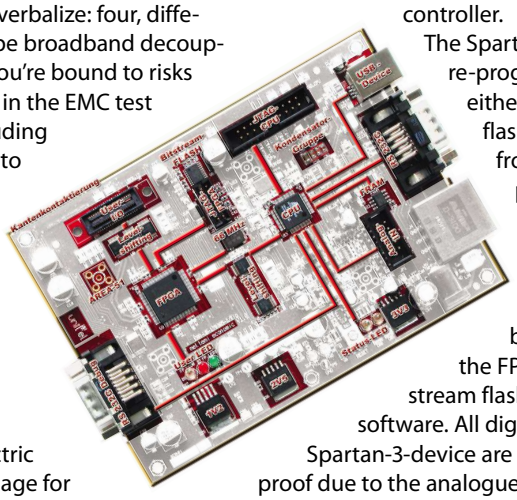


Figure 2: First EMC-measurement result from the absorber hall: indispensable measures to provide the EMC are GND plugs, edge capacitors, edge plating and certain capacitor groups.

Broadband power supply decoupling: That was the first hard nut to crack. The 32-bit-microcontroller needs two voltage levels, the I/O-voltage being 3.3V and the core voltage being 1.8V (the linear regulator is integrated on the chip!). FPGA's from the Spartan-3-family are satisfied with a core voltage of 1.2V and different I/O-voltages of 2.5V or 3.3V – but these only with restrictions. The requirement of providing four LVDS-channels as well fixed this I/O-voltage on 2.5V.

4 different supply voltages to be broadband decoupled

Thus we now have 4, to verbalize: four, different supply voltages to be broadband decoupled. No way out, exept you're bound to risks and love adrenalin kicks in the EMC test facility. Four layers (including GND) out of six were, so to say, used. A mere of two layers have been left for routing the signal traces. By the way, all these signal traces had to be routed impedance defined. Being great fun elaborating the PCB-design.



The requirement an electric strength of 5V input voltage for all signals at the USER I/O plug caused a massive implementation of passive analogue switches with voltage level conversion from the above mentioned 5V to 3.3V (ARM7 CPU) and 2.5V (Spartan-3-FPGA).
The 8-bit bus connection also needed a transceiver for voltage level conversion. Using analogue bus switches has significant advantages. Runtime is a maximum of 200 ps. There is no active interference level into the Vcc-GND-system and the connections are implicit bi-directional. Control lines for change of direction aren't necessary any more. Four analogue inputs of the 10-bit-A/D converter were equipped with external operation amplifiers to fit possible used different sensor elements.

Software with a maximum of flexibility

The regulation of the three different operational voltages was provided by three external linear regulators (3.3V, 2.5V and 1.2V) in SMT and cooled via the two GND planes using thermal vias and the edge plating. The fourth needed operational voltage is generated by the linear regulator integrated in the microcontroller.
The Spartan-3-FPGA can be re-programmed either by serial bit-stream flash or JTAG signals from the ARM7 microprocessor, thus providing the software with a maximum of flexibility and interactional possibilities. A reload of the FPGA out of the bit-stream flash can be forced by software. All digital inputs of the Spartan-3-device are 5V input voltage proof due to the analogue level converter. Additional indispensable measures like GND-plugs, edge plating, capacitor groups combined with the requirement of having only single sided assembly due to the economical point of view increased the time expenses up to sailing close to the wind.
This and the following part makes our New-Year's Pledge 2006 and further, saying "We tried it, we made it, but we will never do it again that way – or only in very extremely exceptional cases", more than understandable. *(cm)*

Squaring the circle II

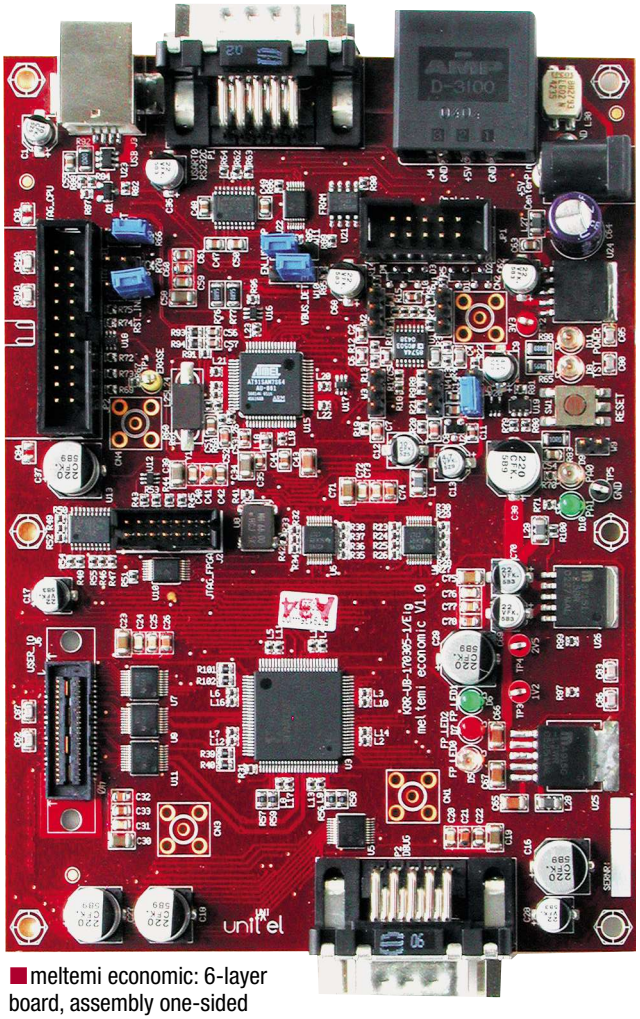
EMV Behaviour and stable Functionality in 6 Layers

With various constructive measures the designers of the 18-layer CPU module CERO and of the 20-layer PCB meltemi were successful realising stable hardware functionality. The high speed platform was successfully established and optimised for stable operation within the recent 7 years. The latest task was, to project the experience gained with high density multilayer boards from the 20 layer level towards the 6 layer level, without loosing too much in respect to EMC behaviour and stable functionality. Additionally it was the goal to achieve single side component placement. At least theoretically a basket of non realizable goals the 6-layer PCB „meltemi economic".

by Gerhard Eigelsreiter

With the perspective to the given task catalogue, the quotation seemed to be quite optimistic, but as an interim solution a goal to reach out for.
Because the catalogue comprised merely the realisation of nearly all measures to reach EMC compatibility within a slim, inexpensive 6-layer PCB construct. Measures, which have been taken during the development phases of the 18 layer CERO CPU Module and the 20 layer meltemi PCB and measures, which have been developed within the last 7 years to secure hardware functionality, measures which could successively be transformed into working hardware. A nearly unsolvable problem: the transformation from 20 layers down to 6 layers, maintaining quality.
For the developer of high speed hardware, one does not have to have excessive fantasies to see oneself confronted with a phalanx of opposition.

- Non the less, the incomprehensive identification of those tasks brings some light into the darkness: 4 power supply systems have to be decoupled in a broadband manner. This concerns the ARM7-CPU with 3.3-V-IO- und 1.8-V Kernel voltages as well as the Spartan-3 FPGA with 2.5-V-IO and 1.2-V-Core Voltages.
Therefore, only 2 layers are left for the placement of the signal lines. Another Constraint is the singe side component placement requirement due to cost factors.
- The provision of 2 symmetrical layers within the PCB with the two power planes positioned outside is mandatory, this demands the application of GND Vias at nearly every position, where signal change planes (signal vias).



meltemi economic: 6-layer board, assembly one-sided

- All the power supply connections to the ARM7-CPU as well as to the Spartan-3 FPGA have to be decoupled via chokes with adequate ohmic components (sums up to 24 chokes).
- Nearly all signal lines are realized in an impedance controlled manner (50 Ω).
- Furthermore, 4 LVDS signal line pairs (100 Ω differential) enhance flexibility of this board level product in the case of increased interconnect length requirements, on the other side this requires constant distances within the differential pair, length matching and the realisation of distance design requirements towards single ended signal lines.
- Groups of capacitors, edge plating and edge capacitors have to be considered too. The derivable consequences disqualify at the same time design tools, such as the auto placer and the ▶

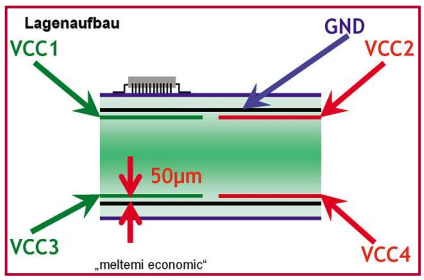


Figure 1:
Stacking of the 6-layer Multilayer Reference Hardware Platform „meltemi economic“

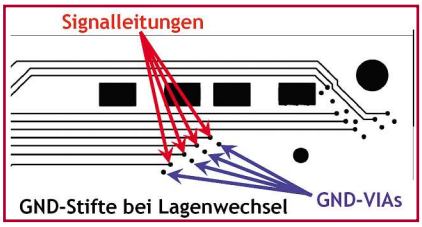


Figure 2:
With each layer change in a signal path, correspondig GND-vias have to be placed as near as possible in the neighbourhood of the signal via.

auto router. Excessive research work was the normal practice, enhanced by long duration design sessions which went often through days and nights.

Terms as e.g. delivery dates and cost pressure became good companions during these sessions. Several examples shall exemplify the chosen solution approaches ...

Layer stacking: Bevor the development of the schematics the layer stacking has to be considered and defined in detail. Half hearted component selection and negligence concerning the layer stacking will exhibit "excellent emission performance", which can be seen at list in the EMC lab. Practically spoken, high EM emission levels cannot be solved any more or can be reduced only within a minor range, after the board has been finished. Cost Intensive re designs are pre-programmed. In figure 1 the layer stacking of this 6-layer reference platform is represented systematically. The two power systems are positioned as inner layers in a symmetric way. Because of the decoupling of 4 supply voltages, the power supply layers had to be split (Vcc1, Vcc2 as well as Vcc3 and Vcc4). Otherwise another 4 layers would have become necessary. The distance between the Vcc and GND layers shows 50 µm only, for the moment this is sort of an optimal realisable approach, also in terms of cost. For usable broadband decoupled ower supply systems, this thickness should in no case be selected above 120 µm.

GND-Vias: 4 layers are already occupied by the power supply system. With only two layers left, the signal lines have to be positioned in the outer layers. Another interesting aspect occurs here: Each layer change of signal (Vias) in the present geometry with different reference GND layers leads to a "wrong" GND layer for the referenced signal return current, if in the neighbourhood (range less 1 cm) no realised interconnect to the relevant GND-layers does exist.
This problem can be solved, if GND-Vias are implemented, which interconnect GND layers. From figure 2 it clearly can be depicted, that the distances to the signal vias should be short as possible, to transduce the signal return path currents as tightly as possible near the signal path. An experienced layouter immediately expects further calamities: The additional space requirement of those GND vias considerably complicates the routing on two layers only, because due to the cost factor, placement of components has to happen on the component side only.

USB connector: With microcontrollers, carrying additional USB peripherals, the routing of differential signal line pairs often is hindered by additional passive components (figure 3). These components should be placed as near as possible beside the CPU pins, as it should be the case with the PLL filter network (fig. 4).In contrast to LVDS line pairs, the differential impedance here is 90 Ω instead of the usually used 100 Ω differential.

Oscillator: Special care should be taken with the signal lines concerning the Xtal Oscillator components (figure 5). Very short signal lines should be chosen. Crosstalk from digital signal lines should be minimized, maybe through the surrounding by additional GND lines.

Filter chokes: All CPU Vcc Pins and also every FPGA Vcc pin is connected to the adequate power planes through low impedance (about 10 Ω) chokes. These components naturally should be again (who wonders) placed as near as possible towards the respective pins.

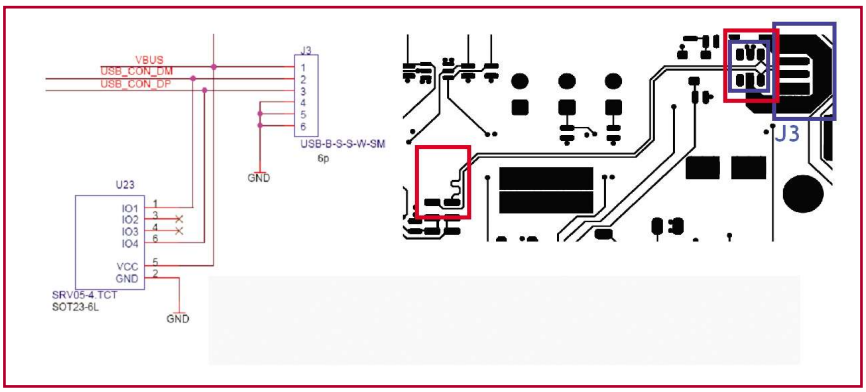


Figure 3:
The length correction generally has to be performed in the area, where the problem arises. (see also red frame on the left side). Also the interconnections to the overvoltage protection array have to be realised corresponding to differential signalling requirements (see also: red and blue frame, right top.)

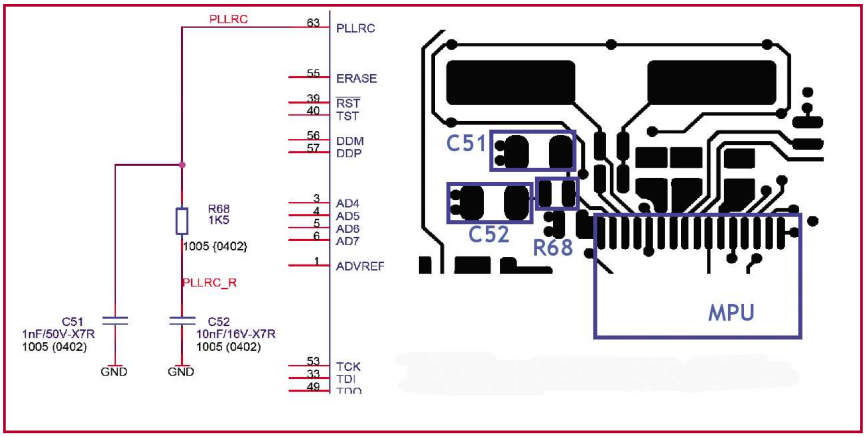
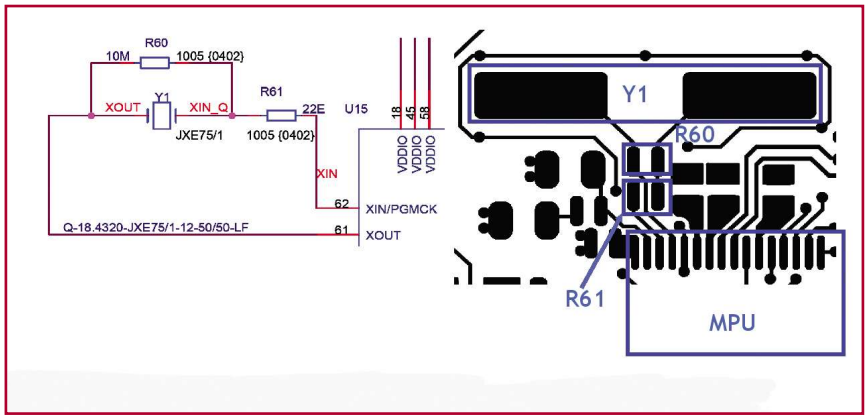
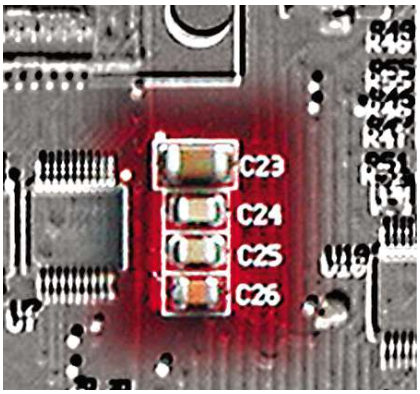


Figure 4:
PLL-filter network of the AT91SAM7S64 ARM7 CPU. On the right side the components in the layout are within the blue frame.

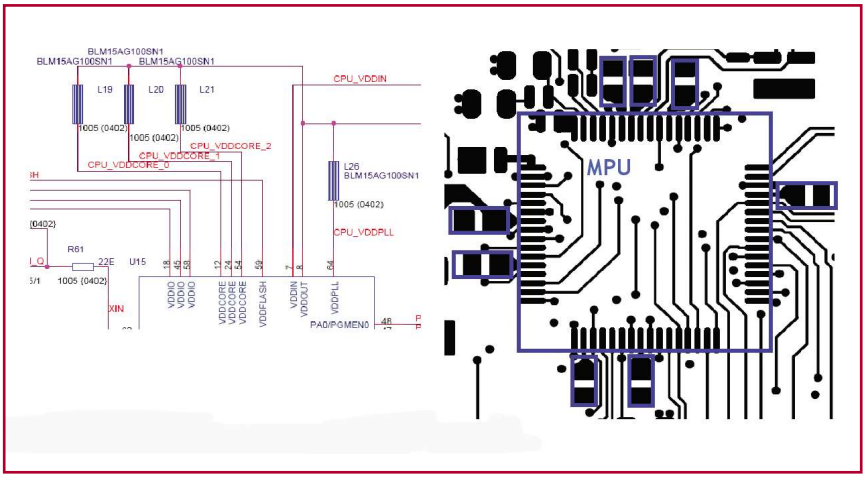


■ Figure 5:
Xtal setup with the ARM-7 CPU Normally implemented 2 capacitors (usually 15 pF) referenced to GND can be eliminated, if a Xtal Oszillator with 12 pF load capacity is used.

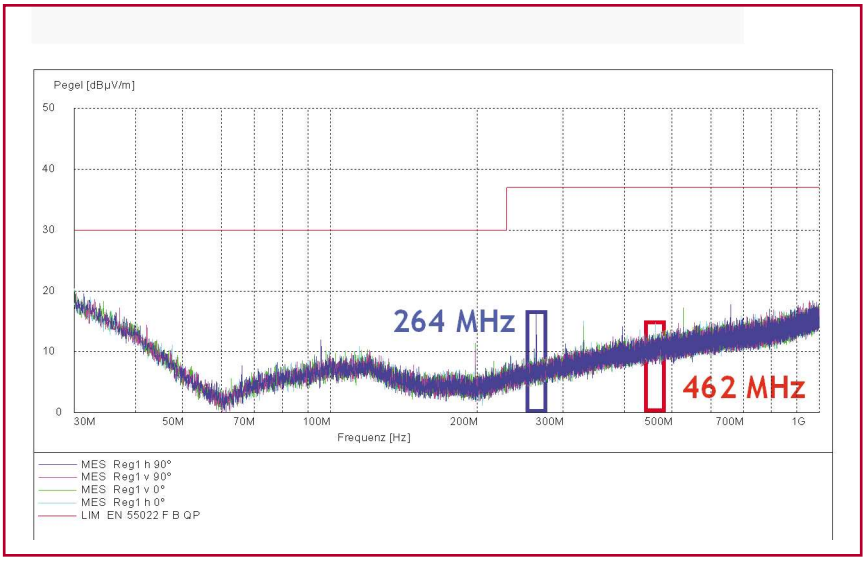


■ Figure 7:
C groups may be placed at a location, where some space is left, if only radii of effectiveness are large enough.

■ **Capacitor groups:** (figure 7) the C groups may be placed in an area, where there is sufficient space available, thanks to their radius of activity. It is recommended, not to place them in the Edge/Corner Areas of the PCB. The C-values of the C groups have to be calculated with adequate programs. The C-values for the reference platform were derived from results, which have been calculated with the software tool „Silent“ (see page 80).
Mere two signal planes were available on the meltemi economic-board to materialize signal integrity and to realize measures for a EMC-compatible design. The EMC Test results nevertheless made up for all the pains and efforts involved in the design- and layout process. But: the planned realisation time horizon was largely stressed and exceeded. There existed several reasons for the increased realisation period.
A double sided component placement combined with 2 additional signal layers would already result in a significant reduction in the layout realisation phase. From a commercial and cost point of view, this 6 layer design only makes sense for high production quantities.
On the other hand, it should not be forgotten, that in our case we wanted to establish a 6 layer reference platform. With the goal, to provide ways for solutions for many different application requirements, and also to transfer and initiate some ideas towards more complex PCB constructs.
Anyone, who does not want to invest into development time requirements to develop an own project from scratch, can buy the platform and can go into details through the documentation given along, which includes also schematics and the PCB payout (see page 80). ■



■ Figure 6:
Here in the schematics, only part of the chokes shown on the right hand side (in bue box) can be seen. All 8 power supply pins of the ARM7-CPU have to be decoupled separately.



■ Figure 8:
EMC emission spectral measurement, „meltemi economic“: 4th harmonic (blue box) and the 7th harmonic (red box). The results are excellent and correspond to expectations.

Chapter 10

The optimized multilayer stack-up

Philosophical Voltages I

In part 8 and 9 we introduced the "meltemi" device: 32-Bit micro controller, flexible I/O structure und free programmable hardware accelerators or re-programmable logic (Spartan-3-FPGA) significantly expand the possible fields of application for the hardware. Opposite to the "meltemi"-board with 20 layers for "meltemi-economic" 6 layers had to be sufficient – without having delimiting effects on functional safety and stability on the hardware. To realize such a stack-up, simple but optimised to smallest details, means to compete with highly complex coherences. The result are common construction principles and operating strategies for future circuits.

by Arnold Wiemers

Known as a principle and worthwhile goal in engineering applying the necessary and sufficient in a industry product. Albert Einstein is cited with "Everything should be made as simple as possible, but not simpler!".
One clue in the concept of Gerhard Eigelsreiter is finding a optimal solution for a complex problem. In his lectures "CERO" (see page 62ff and "meltemi" the sentence is to be find "Simple simplicity requires complex complexity". Hearing this statement spontaneously you get the intuitive feeling having met one of the elementary cognitions of present philosophy.
Is it possible that this kind of reflection can touch such a simple product as a PCB? Is the concept for a stack-up probably underlying the principles of the theory of cognition?
Well, indeed yes. It is incidental that a simple but optimised stack-up requires a complex theoretical and practical environment.

The strategic concept for the high speed CPU meltemi

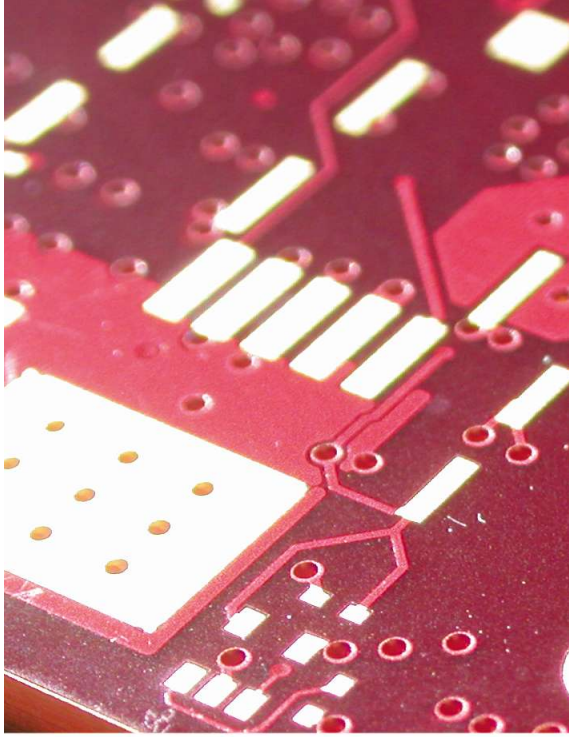
The "meltemi"-board exists in two versions. The high layer count first version with 20 layers is designed for a high speed application with a data throughput in the Gbit range. Regarding the task the layer count seems to be appropriate. Was it designed according to the concept "the more the better"?
However, the 20-layer board meltemi was verified by practise. Quod erat expectandum.
Behind the concept of meltemi board four concrete statements are found which form the requirements for an effective multilayer stack-up and are standing for a stabile and safe function of a device:

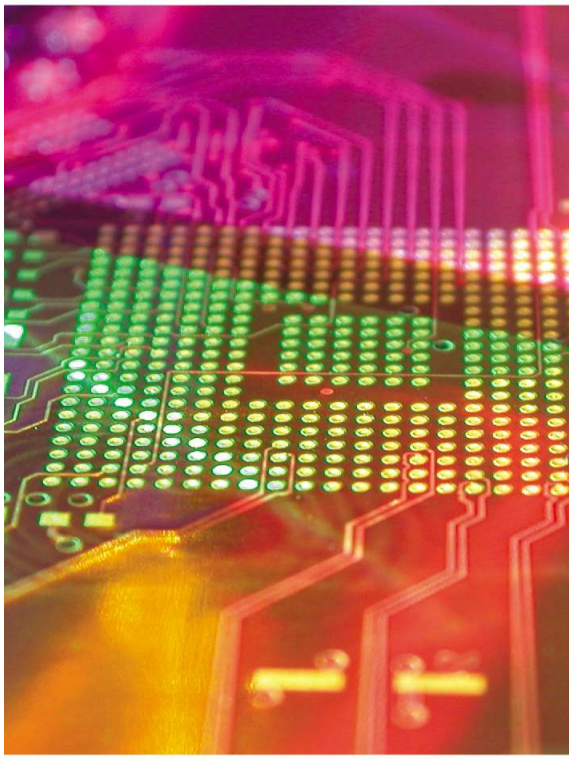
1. Decoupling
The standard decoupling of an electronic circuit can be provided broadband through capacitive power planes with a layer distance of 50 µm. Additionally only local capacitor groups have to be added.

2. EMC-immission/-emmission
EMC-emissions and/or the interference susceptance of a device is reduced drastically by plating the PCB edge.

3. Signal-integrity
Definite GND references for back current paths optimise signal-integrity. Having several signal layers the GND references must not overlap.

4. Self-interference
Interferences of a device caused by it's own Vcc planes ("Internal EMC") is reduced to a minimum if the Vcc planes are shielded by flanking GND planes against the signal layers.





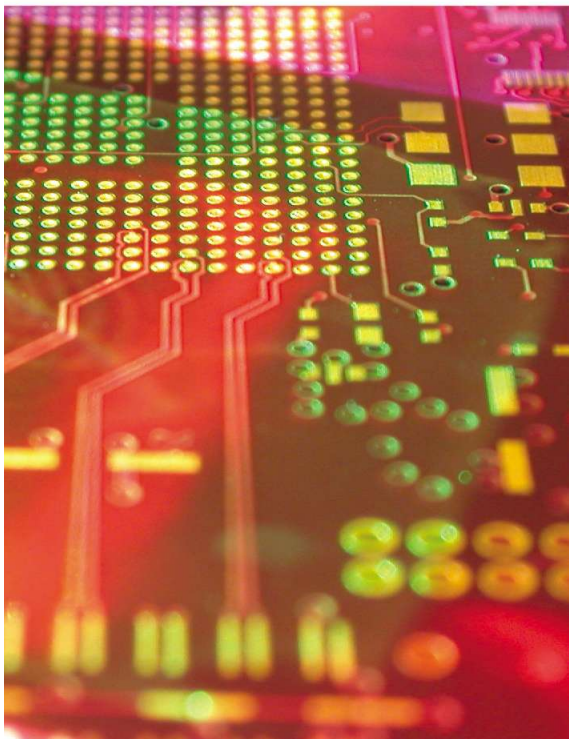


Chart 1	Variant 1	Variant 3	Variant 3	Variant 3
Layer 1	SIGNAL	SIGNAL	SIGNAL	GND
Layer 2	SIGNAL	GND	GND	SIGNAL
Layer 3	VCC	VCC	SIGNAL	VCC
Layer 4	GND	SIGNAL	VCC	SIGNAL
Decoupling	good	good	bad	bad
EMC	bad	bad	bad	bad
Signal-integrity	bad	bad	good	bad
Self-interference	moderate	moderate	moderate	high

Chart 1: 4-layer stack-ups are not effective – exemplarily four stack-up variants have been examined and analysed in regard of the four statements.

Chart 2	Variant 1	Variant 2	Variant 3	Variant 4	Variant 5	Variant 6
Layer 1	SIGNAL	SIGNAL	GND	SIGNAL	SIGNAL	SIGNAL
Layer 2	SIGNAL	GND	VCC	GND	GND	GND
Layer 3	VCC	VCC	SIGNAL	VCC	VCC	VCC
Layer 4	GND	VCC	SIGNAL	SIGNAL	GND	GND
Layer 5	SIGNAL	GND	VCC	GND	Not used	SIGNAL
Layer 6	SIGNAL	SIGNAL	GND	SIGNAL	SIGNAL	SIGNAL
Decoupling	good	good	good	good	good	good
EMC	bad	good	moderate	moderate	good	good
Signal-integrity	bad	good	bad	good	good	bad
Self-interference	moderate	low	high	moderate	low	low

Chart 2: 6-layer boards offer a minimised solution – exemplarily six stack-up variants have been examined and analysed in regard of the four statements

Pure minimalism: "meltemi econmic"

Well, as stated before, everybody can deal with 20 layers. To clarify, whether the prognosticated statements on the physical qualities probably may have a universal validity the second version of "meltemi" was projected, the device "meltemi economic".

As if the technical challenges weren't enough an additional complication should have been tackled with "meltemi economic". The clue was to find the minimum requirement that ensures the verification of the four statements above. Provided the assumption that such a minimum requirement exists at all however. This assumption is elementary. If it could be proved that there is a minimum requirement existing than all stack-up variants beyond this minimum requirement don't satisfy the predicted physical properties. These stack-up variants would not be optimised or in extreme cases, depending on the layer distribution, not even usable at all.

For everyday PCB business this reflection inaugurates a new dimension. In the real world of PCB manufacturing for material logistic, machine investments and staff education concepts long term planning security is necessary. The reliable statement with a verified background which PCB product will be the future and which one will be useless is a huge strategic advantage now and henceforth. ▶

Four Requirements for a fail-safe function

The meltemi project is based on four factors which can be considered as requirements for an effective stack-up and a fail-safe and stabile function of the device:

■ **1. Decoupling**

The standard decoupling of an electronic circuit can be provided broadband through capacitive power planes with a layer distance of 50 µm. Additionally only local capacitor groups have to be added.

■ **2. EMC-immission/-emmission**

EMC-emissions and/or the interference susceptance of a device is reduced drastically by plating the PCB edge.

■ **3. Signal-integrity**

Definite GND references for back current paths optimise signal-integrity. Having several signal layers the GND references must not overlap.

■ **4. Self-interference**

Interferences of a device caused by it's own Vcc planes ("Internal EMC") is reduced to a minimum if the Vcc planes are shielded by flanking GND planes against the signal layers.

The evaluated stack-up variants

The term "stack-up variant" in this case means exclusively the distribution of signal layers and power planes within a given physical stack-up. The only assumption is that three qualities of layers named SIGNAL, GND and Vcc exist and that each quality uses a complete layer and that each appears at least once in the stack-up. Subsequently these variants resulting from different possible combinations are evaluated in regard of the four statements above.

Decoupling is rated as "good" if Vcc and GND are put on adjacent layers because a plane capacitor is achievable by minimising the layer distance. A "bad" rating is given if Vcc and GND are not lying on adjacent layers because thus capacitive effect are impossible by means.

EMC is rated "good" if all inner SIGNAL layers are covered by GND layers and the Vccplanes are located inside the multilayer thus having the possibility to be shielded by edge plating. A SIGNAL layer is rated "moderate" when a Vcc plane is lying next to it. A "bad" rating is given if Vcc isn't covered on both sides by GND and when it can't be shielded by edge plating.

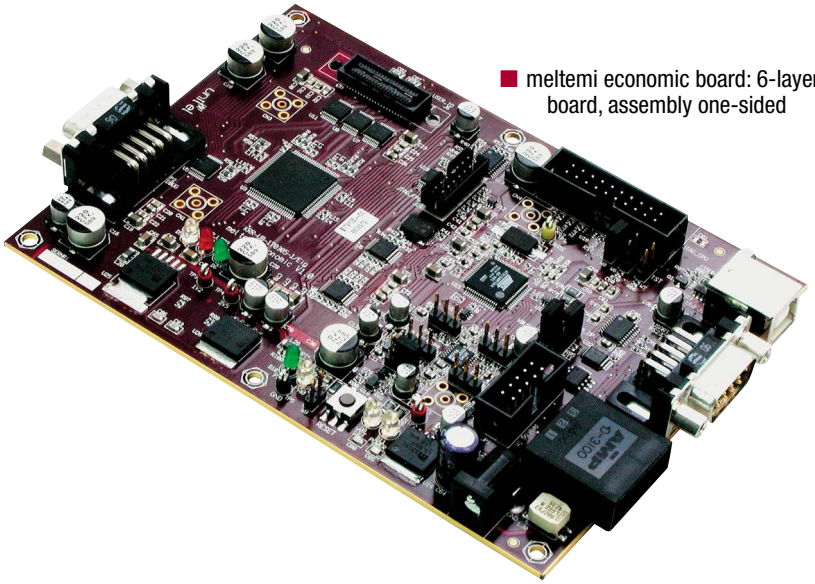
Signal-integrity is rated "good" if each SIGNAL faces a GND as adjacent layer. A "bad" rating is given if beween a SIGNAL layer and it's GND second SIGNAL layer or a Vcc plane is placed.

Self-interference is rated "low" if all SIGNAL's are shielded from Vcc by GND. A "moderate" is given if only one SIGNAL layer is affected, self-interference is considered "high" if more than one SIGNAL layer is affected.

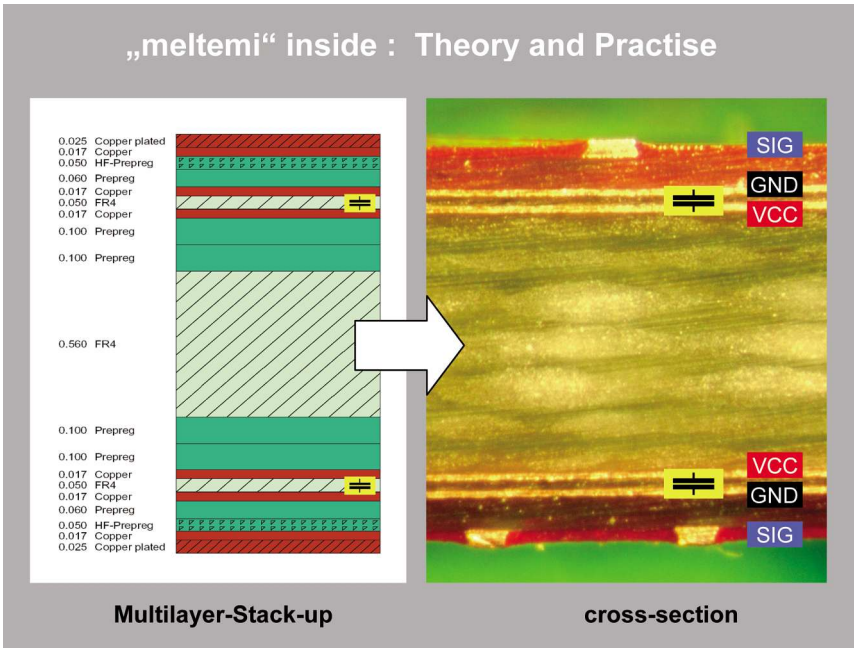
The evaluated stack-up variants

The term "stack-up variant" in this case does not mean physical stack-up but exclusively the distribution of signal layers and power planes within a given physical stack-up. Essentially the focus is put on uncomplicated combinatory aspects. The assumption is that only the three qualities of layers named SIGNAL, GND and Vcc exist and that each quality uses a complete layer and that each appears at least once in the stack-up.
Subsequently these stack-up variants resulting from the different combinations are evaluated in regard of the four statements above.

Decoupling is rated as "good" if Vcc and GND are put on adjacent layers because a plane capacitor is achievable by minimising the layer distance. A "bad" rating is given if Vcc and GND are not lying on adjacent layers because thus capacitive effect are impossible by means.
EMC is rated "good" if all inner SIGNAL layers are covered by GND layers and the Vcc planes are located inside the multilayer thus having the possibility to be shielded by edge plating. A SIGNAL layer is rated "moderate" when a Vcc plane is lying next to it. A "bad" rating is given if Vcc isn't covered on both sides by GND and when it can't be shielded by edge plating.
Signal-integrity is rated "good" if each SIGNAL faces a GND as adjacent layer. A "bad" rating is given if beween a SIGNAL layer and it's GND second SIGNAL layer or a Vcc plane is placed.
Self-Interference is rated "low" if all SIGNAL's are shielded from Vcc by GND. A "moderate" is given if only one SIGNAL layer is affected, self-interference is considered "high" if more than one SIGNAL layer is affected.



meltemi economic board: 6-layer board, assembly one-sided



The stack-up for meltemi economic consists of two 50 µm cores with 17 µm copper coated. To bridge the distance between the two Vcc planes an etched 560 µm core was built in. All signals were routed on the two external layers.

4-layer stack-up are not efficient in regard of technical requirements

Exemplarily four stack-up variants are examined for the 4-layer board type. The evaluation of these variants considering the four known statements is set up in chart 1.
The disadvantages are clearly recognisable. Against the background of the upcoming technological requirements an appropriate stack-up with 4 layer is not feasible. Thus resulting in the fundamental conclusion that 4 layer boards will not be usable for future applications.

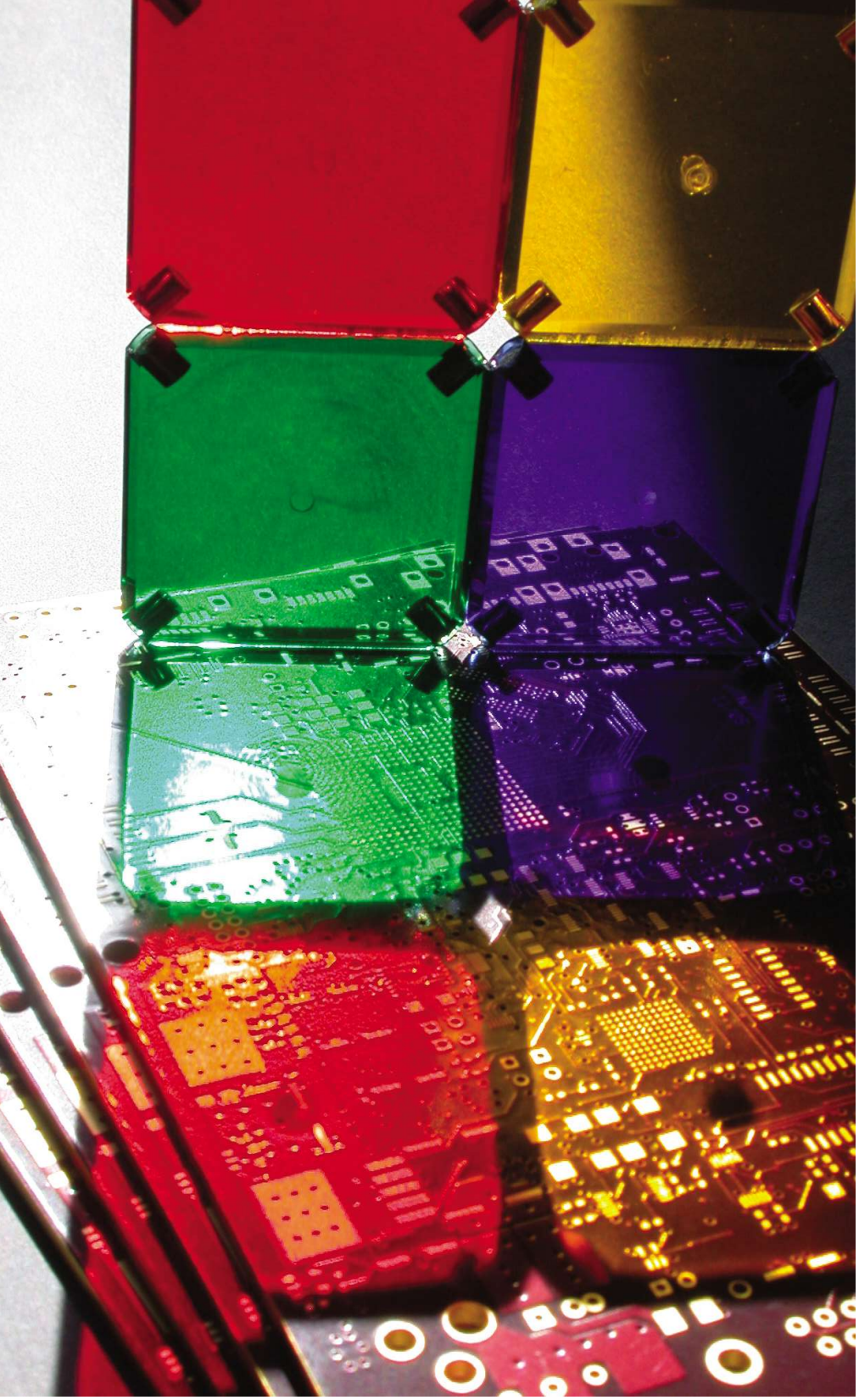
6-layer stack-up offer a minimised solution

For the evaluation of the 6-layer board exemplarily six distribution variants are examined. Against the background of the before described four statements the evaluation of these variants is given in chart 2. Variant 2 represents the optimum for a 6 layer board in all parameters. But bought dearly restricting the routing to only two signal layers. It is the stack-up used for meltemi economic.
All other variants show disadvantages. I.e. variant 1, 3 and 4 all show signal layers which face a Vcc plane thus having impact on signal-integrity.

The layer count allways has not to be an even number

One exemption is variant 5. Not using layer 5 the properties in total are better than in the nearly identical variant 6. As well here we have to abandon a (possible) signal layer. But the focus is on something different. It has never been a precaution that all n layers of an n-layer board have to be used or respectively that the layer count always has to be an even number.

Conclusion:
All hitherto existing presumptions are simple in nature. Further requirements on material or via strategy common in practise are not considered. But already now we get the idea that probably the typical 4-, 6- or 8-layer board may not exist. *(cm)* ■



In the first chapter we got already an idea that the typical 4-, 6- or 8-layer board probably might not exist. This chapter in which the 8- and 10-layer board are described affirms the truth of the statement. With classical construction principles an optimized stack-up demonstrably isn't always achievable. However the success of the "meltemi" project is not drawn back on the stack-up of the multilayer-system alone. While the deliberately placing of GND spikes improves signal-integrity the plating of the PCB edges has a big share in EMC stability.

The optimized multilayer stack-up

Philosophical Voltages II

by Arnold Wiemers

In the first chapter of "Philosophical voltages" Gerhard Eigelsreiter was cited with the statement "Simple simplicity requires complex complexity" in reference to his project "meltemi". Against the background of the properties of the "meltemi economic" board fundamental strategic aspects for constructing multilayer-systems have been discussed. As criteria four statements were defined to evaluate decoupling, EMC-immission/-emission, signal-integrity and self-interference. The definition of these four statements from the first chapter has been summarised on page 43. The present second chapter concentrates on 8- and 10-layer boards. As a reference for the performance of multilayer-systems the GND spikes of the "meltemi economic" and the shielding of power supply systems by edge plating of PCBs are described.

8-layer boards rarely are optimised

Exemplarily six stack-up variants are examined for the 8-layer board type. The evaluation of these variants considering the four known statements is set up in chart 1.

The best solution in form and content is to be found in variant 2. It is surely interesting that the capacitive properties of this possible 8-layer board are about 25% less than those for the optimised 6-layer stack-up being constructed for "meltemi economic" (refer to chapter 1). ▶

Strategically variant 2 is the best solution. Incidental are four signal layers and four power planes. Considering that the distances between layer 2, 3 and 4 are at the minimum of 50 µm an asymmetrical stack-up has to be assumed often leading to disadvantages or limitation for PCB production, because many PCB manufacturers don't accept asymmetrical stack-up's. Admissible is also variant 5 with the limitation that signal layer 4 is influenced through Vcc layer 3. Surprisingly 8-layer boards are subject to restrictions respectively limitations. More likely had been that more layers globally mean more capable and effective combinations. However in practice the possible layer combinations are not optimised.

10-layer stack-up's offer manifold solutions

For the 10-layer board type as six stack-up variants exemplarily are examined. The evaluation of these variants considering the four known statements is set up in chart 2. Only from 10 layers on due to the combination possibilities for power plane and signal layer distribution success promising solutions are again to be expected.

Apart from construction detail (i.e. layer distances, basic material) of the multilayer-system functional successful solutions (see variant 1 and 2) can be created by combining 4 to 5 signal layers with the necessary power planes. Due to the requirements for multilayer-systems to meet additional demands (heat dissipation, mechanical stability, current carrying capacity…) it is obvious why multilayers consisting of more layers seem to be "en vogue". At the moment the prognosis that multilayer-systems with 8 or 10 layers will determine the PCB technology of the coming years seems to fulfil.

Chart 1

	Variant 1	Variant 2	Variant 3	Variant 4	Variant 5	Variant 6
Layer 1	SIGNAL	SIGNAL	SIGNAL	GND	SIGNAL	SIGNAL
Layer 2	GND	GND	SIGNAL	VCC	GND	GND
Layer 3	VCC	VCC	GND	SIGNAL	VCC	SIGNAL
Layer 4	SIGNAL	GND	VCC	SIGNAL	SIGNAL	VCC
Layer 5	SIGNAL	SIGNAL	VCC	SIGNAL	GND	SIGNAL
Layer 6	VCC	SIGNAL	GND	SIGNAL	SIGNAL	SIGNAL
Layer 7	GND	GND	SIGNAL	VCC	GND	GND
Layer 8	SIGNAL	SIGNAL	SIGNAL	GND	SIGNAL	SIGNAL
Decoupling	good	good	good	good	good	bad
EMC	moderate	good	moderate	moderate	moderate	bad
Signal-integrity	bad	good	bad	bad	good	bad
Self-inteference	high	low	low	high	moderate	moderate

Chart 1: 8-layer stack-ups subject to limitations. The possible combinations in practise are not effective.

Chart 2

	Variant 1	Variant 2	Variant 3	Variant 4	Variant 5	Variant 6
Layer 1	SIGNAL	SIGNAL	SIGNAL	GND	SIGNAL	SIGNAL
Layer 2	GND	GND	SIGNAL	VCC	GND	SIGNAL
Layer 3	VCC	VCC	GND	GND	VCC	GND
Layer 4	GND	GND	SIGNAL	SIGNAL	SIGNAL	SIGNAL
Layer 5	VCC	SIGNAL	GND	SIGNAL	GND	VCC
Layer 6	GND	GND	VCC	GND	SIGNAL	SIGNAL
Layer 7	SIGNAL	SIGNAL	GND	VCC	SIGNAL	SIGNAL
Layer 8	SIGNAL	SIGNAL	SIGNAL	SIGNAL	GND	SIGNAL
Layer 9	GND	GND	SIGNAL	SIGNAL	SIGNAL	SIGNAL
Layer 10	SIGNAL	SIGNAL	SIGNAL	GND	SIGNAL	SIGNAL
Decoupling	good	good	good	good	good	bad
EMC	good	good	good	moderate	moderate	bad
Signal-integrity	good	good	bad	bad	bad	bad
Self-interference	low	low	low	moderate	moderate	high

Chart 2: Only from 10 layers on due to the combination possibilities for power plane and signal layer distribution success promising solutions are to be expected

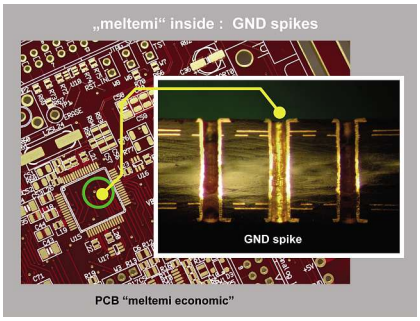


Figure 1: At discrete positions in the design of "meltemi economic" GND spikes are placed (here recognizable as not being covered with solder mask). The cross-section was made through three vias in the position marked by the green circle.

GND spikes and Faraday cages in the design

The general stack-up of meltemi economic has been elucidated already. Two contributions still due. The minimalist stack-up wouldn't have been sufficient. The deliberate placing of GND spikes improves signal-integrity. Due to this additional and individual impact on back currents by design composition the circuit is restrained and controlled.

EMC stability is mainly drawn back on the edge plating of the PCB borders. Naturally it is presumed that an appropriate design contributes to the technical properties. To achieve an effective shielding the GND planes, in the example of "meltemi economic" it concerns the layers 2 and 5, have to be lead to the edge of the PCB. By electrical contact of the GND planes over the plated PCB edge a (under faraday aspects) hermetically closed room is built. The inner Vcc planes on the layers 3 and 4 are designed with sufficient distance as in figure 2 clearly visible. The result are Vcc planes which are entirely embedded and shielded by GND planes plus plated PCB edge.

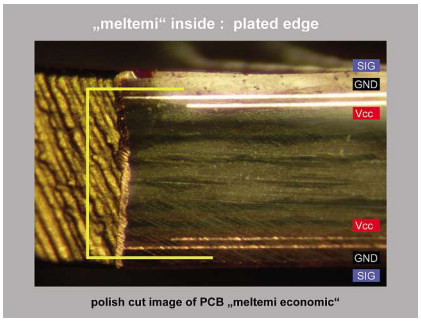


Figure 2: Left handed in the cross-section the PCB edge (immersion gold above Ni and Copper) is to be seen. The GND planes, layer 2 and 5, reach the border of the PCB and are electrically connected via the plated edge.

Conclusion:

The achievement in designing meltemi economic consisted among others in constructing a high performance multilayer even with reduced layer count. Such a solution anyhow is hard-faught. The reduction from 20 layers to (maybe) 10 and then to 6 layers seems to be economically plausible. Technically it is an extraordinarily demanding challenge. A solution like this isn't just decided, this calls for proficiency. Kudos to you: the designer and the constructor are the ones to collect the compliments.

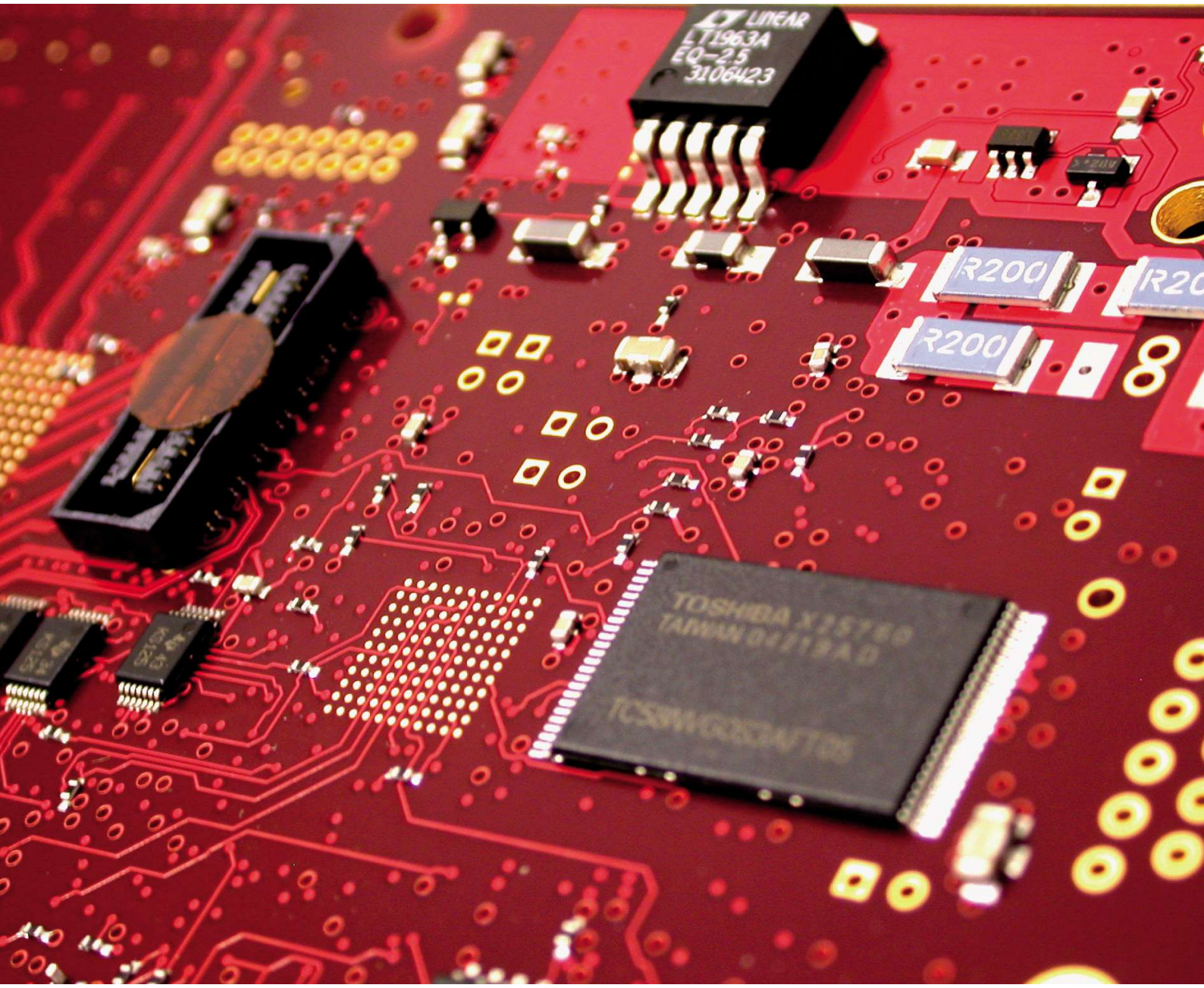
Well, it's adopted as it stands: For "simple" devices the environment get more and more complex as meltemi economic dramatically proves. It is obvious that solely the alliance of disciplines "Circuit Design" plus "CAD-Design and Construction" plus "PCB Production" plus "Device Assembly" will be successful. *(cm)*

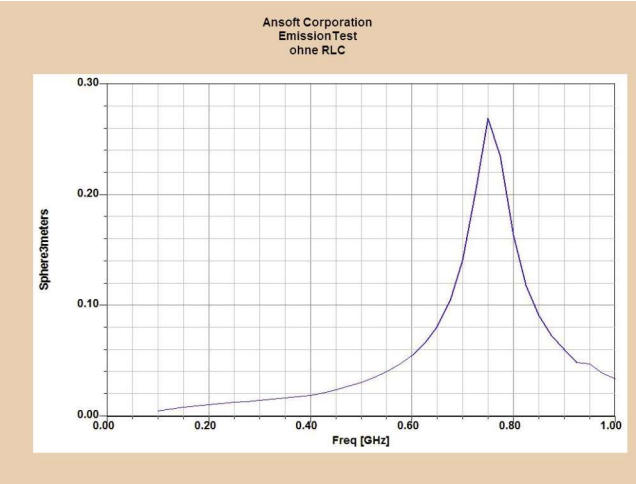
Terminating power plane systems

The Edge Capacitor

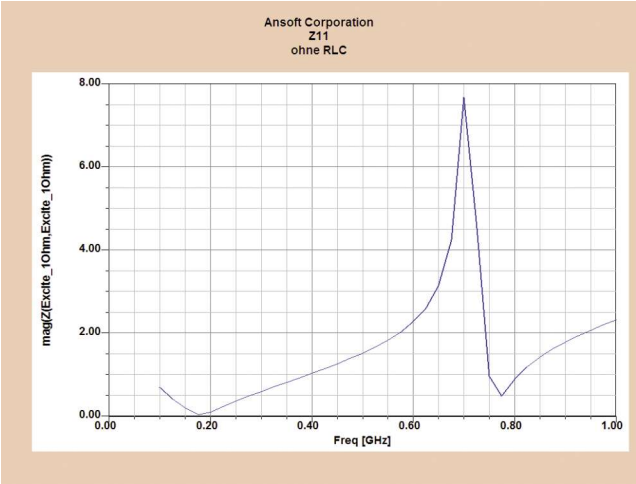
The need to model power plane systems as multi-dimensional lines has already been demonstrated in [1]. Design engineers who implement this strategy will discover a wealth of benefits for decoupling and EMC. However, the distributed nature of these systems also causes unwanted resonances. This side effect requires appropriate countermeasures in order to maintain solid power integrity and sound EMC characteristics.

by Nils Dirks





■ Figure 1:
"Emission Test" – Just above 700 MHz, we find a pronounced maximum that can be easily identified as the half-lambda mode



■ Figure 2:
System's input impedance at the generator's location; the high impedance at the open "end" of the line is transformed into an "open" over a distance of half-lambda. This "open" appears as a pronounced maximum of the magnitude of impedance.

▶ When designing planar power systems in printed circuit boards (also referred to as "power planes"), design engineers must perform multiple tasks: Ensuring a stable supply voltage and providing (preferably broadband) decoupling are two of the most significant of these tasks. The latter is required to efficiently control high-frequency noise, while a stable supply voltage ensures sufficient provision of energy to the integrated circuits. This paper will describe one specific means of efficiently controlling high-frequency noise.
Again, there are two major reasons for controlling the noise level within such power planes: First of all, the attached consumers (such as integrated circuits) depend on clean supply voltages to ensure reliable and error-free operation. Secondly, the considerable size of such power systems turns them into rather efficient antennas that directly emit high-frequency noise – a most undesirable effect!

Modern digital electronics emit high levels of broadband noise

It can be shown that problematic interference levels arise particularly when resonators have inadvertently formed within the power system. These resonators can be easily excited to their respective resonant frequencies, which (due to their quality factor Q) enables them to reach substantially higher interference levels than would have been possible without such resonances. These resonators may form when capacitors are shunted without much thought [see 2]– capacitors that resonate by means of various parasitic inductances or by cavity resonances within the primarily two-dimensional plane system. When we consider the question of what excites these resonators, the clock net is usually the main suspect, because its various harmonics can be found almost everywhere in the circuits. Avoiding unfavorable clock rates can, in fact, represent one first step towards controlling interference levels. Nevertheless, due to the high-frequency content found in both the signal and supply-current pulses, modern digital electronics emit high levels of broadband noise within the signal nets and the supply nets. Since they cover frequency ranges spanning several hundred megahertz, spectral components can arise at almost any frequency, which can result in excitation of virtually any resonator. Therefore, one essential step in the design of such power systems is the successful avoidance of parasitic resonators across a broad range of frequencies!
That is no easy task: Line-type or cavity-type resonances are an inherent property of any non-lumped structure, because such structures are able to accommodate standing waves. One prerequisite for the formation of standing waves is reflection. That is why some have suggested terminating the two-dimensional lines formed by such power planes with their characteristic impedance [see 3].
Terminating one-dimensional lines is a rather straightforward approach to removing reflections: We can easily terminate a 50 Ω coaxial cable, for instance, by placing a 50 Ω shunt at the end of the cable: This shunt will completely absorb any waves traveling down this waveguide; no reflections occur, and no resonances can be observed. Nonetheless, for a power system consisting of a ground plane and a power plane, there is no obvious "end" of the line, and it is not easy to determine the resistance value that is required for proper termination.
The purpose of terminating a waveguide is to remove any impedance discontinuities along the waveguide, because any change of impedance causes reflections. When we examine the power system as waveguide, we find such discontinuities all along the edges of the planes, which requires distribution of adequate shunts along these edges in order to provide proper termination.
For this reason, to achieve a well-designed power system, we would have to attach multiple resistors (with a value of a few tenths of an ohm) along the edges of the system. Although such measures are not suitable for practical power systems due to power-consumption issues, they would effectively mitigate resonances. In order to solve the power consumption issue, some have suggested the application of what is known as "RC termination": Here, a resistor and a capacitor are combined in series and used instead of a single resistor, which effectively solves the DC problem. However, due to the well-known narrowband properties of real-life capacitors, this type of

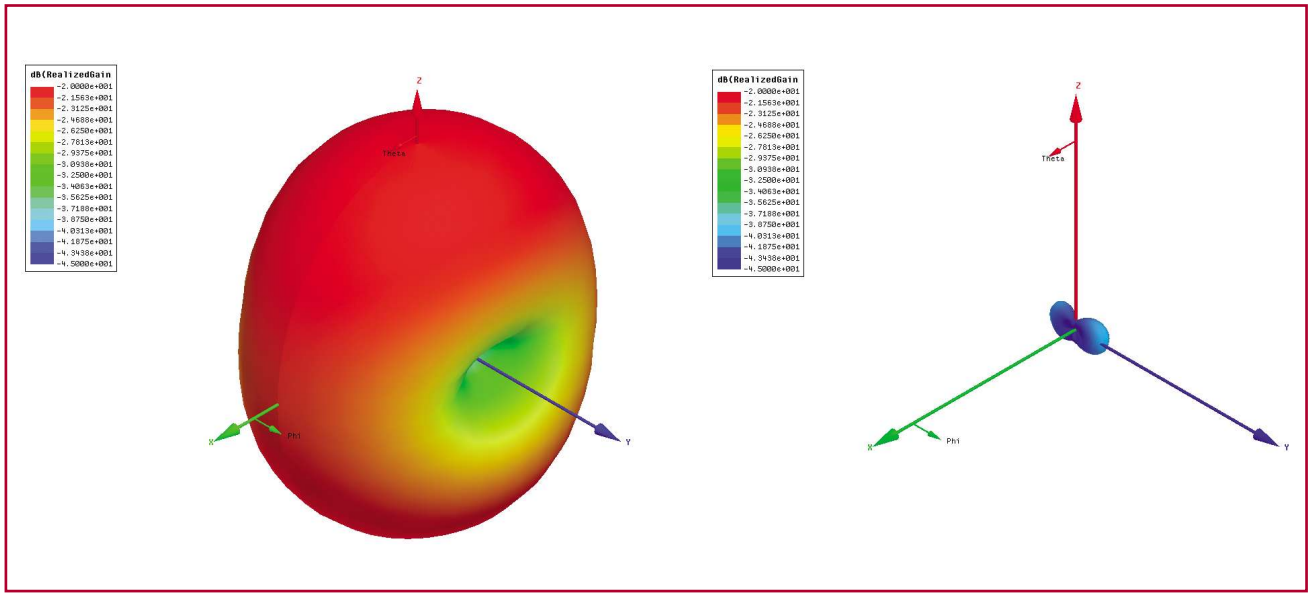


Figure 3:
Comparison of the far field radiation at this frequency for the cases with and without termination; improvement in the order of magnitude of 20 dB

termination does not permit broadband characteristics. In light of this drawback, providing proper termination by means of lumped elements seems impossible. It would appear that genuine broadband solutions are indispensable [4].

The type of termination can be used to effectively improve EMC

Despite these considerations, this paper will nonetheless show how this type of "termination" can be used to effectively improve EMC by intelligently adjusting the appropriate parameters. To study the characteristics of such a "termination," a four-layer PCB has been setup using HFSS V.10.1 to accurately simulate the high-frequency behavior: The edges are 8 and 10 cm long; layers one and four are unused; layers two and three accommodate the Vcc and GND planes respectively, and they are separated by 200 µm of FR4. At position (10 cm, 4 cm), a generator that excites the power system was installed, which simulates a high-frequency noise source. In a practical PCB, this could be an integrated circuit that introduces such noise through the broadband spectral content of its current pulses. The emissions of this setup were then examined in order to identify possible characteristic noise frequencies. Figure 1 shows the "Emission Test," in which the maximum strength of the electric field can be seen at a distance of 3 m for each given frequency.
Just above 700 MHz, we find a pronounced maximum that can be easily identified as the half-lambda mode. The 10 cm extension of the plane system accommodates standing waves; a line-type resonator is in operation. When we observe the system's input impedance at the generator's location, the expected transformation becomes obvious: The high impedance at the open "end" of the line is transformed into an "open" over a distance of half-lambda. This (lossy) "open" appears as a pronounced maximum of the magnitude of impedance in figure 2. This very clearly reconfirms the immediate connection between resonance and emission. In our case, however, this also represents the RC termination's "comeback": Although it is still a narrowband solution, by picking the right values, we may well hope to achieve an improvement, because the bandwidth of the problematic resonance is also narrow. Now we install an RC series combination between the power plane and GND plane at position (0 cm, 4 cm), thus terminating the line's "open end." The RC termination must be designed to achieve a purely resistive character at the line's resonant frequency, because true termination must not contain any reactance. This obviously holds true for the series resonant frequency for the RC combination. Knowing its parasitic inductance, we can easily calculate the required capacitance using

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

the Thomson formula . If we ensure that the RC combination's total resistance equals the characteristic impedance (Z0) of the planar line (the power system), it is "properly terminated" for at least this specific frequency. Although the selected value of 0.1 Ω is probably less than the characteristic impedance (which means that the termination is not perfect), we can observe a substantial improvement: When we compare the far field radiation at this frequency for the cases with and without termination (figure 3), we see an improvement in the order of magnitude of 20 dB!

The RC termination reveals series resonant behavior

The RC termination reveals series resonant behavior. For this reason, it is mainly capacitive below, and mainly inductive above, its series resonant frequency. The power system's line resonance is a shunt resonance, and it behaves in the opposite manner. This clearly suggests that adding the RC termination means adding two new resonators, one above and one below the original resonant frequency. The emission test in figure 4 shows the emission reduction at the original resonant frequency as well as the two newly gained emission maxima at 670 MHz and 825 MHz. These maxima, however, are almost as pronounced as the original maximum! The obvious cause for this is the relatively high quality factor of the RC series resonator, which suggests that it would make sense to increase the ▶

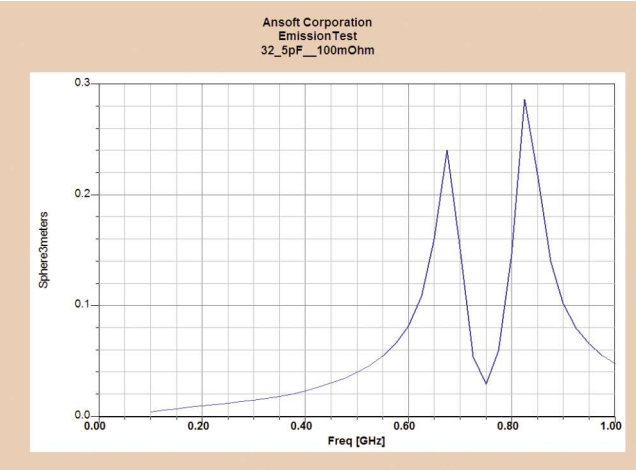


Figure 4:
Emission reduction at the original resonant frequency as well as the two newly gained emission maxima at 670 MHz and 825 MHz (RC terminations, R = 0.1 Ω)

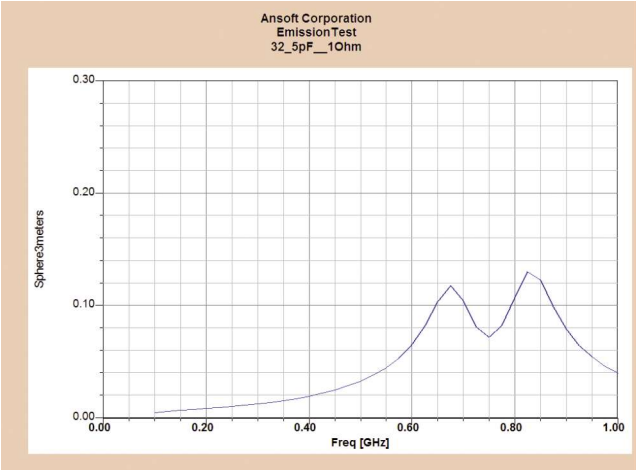


Figure 5:
Effect of increasing the resistor from 0.1 to 1 Ω. The magnitude of emission at the original resonant frequency has regained about 10 dB while both side resonances have lost some 5 dB.

resistive portion. At this point, we need to find the right trade off between sufficient loss for the reduction of the quality factor on one hand, and a resistor value that provides effective termination of the planar line on the other hand. Figure 5 shows the effect of increasing the resistor from 0.1 to 1 Ω: The magnitude of emission at the original resonant frequency has regained about 10 dB while both side resonances have lost some 5 dB. In total, an improvement of roughly 6 dB remains compared to the unterminated system. Using multiple RC terminations along one or more edges further improves the situation, because it facilitates termination of the line with the appropriate resistance while maintaining sufficient total loss.

Understanding of the real-life characteristics of planar power systems is important

When using very thin laminates – such as the ones used for the meltemi-boards – choosing the proper capacitors may render the resistor completely obsolete. In this case, the capacitor's dielectric loss provides efficient termination of the line.
The measurement in Fig. 6 shows a value that is proportional to the magnitude of impedance as measured at port CN1 within the meltemi economic board's 1V2 FPGA core power system. The green trace represents the unpopulated board, and the red trace reflects the situation after adding a small capacitor group (82 pF and 120 pF) at position C87. Applying simple arithmetic makes it possible to evaluate the impedance values, and it reveals a reduction of the shunt resonance at 675 MHz by about 40%. However, adding any additional resonators (such as an RC termination or a capacitor) can always result in additional resonances, depending on its position within the system and on the other components that are installed. This may lead to additional shunt resonances within the power system. That can not be tolerated from an EMC point of view, and it requires accurate investigation of the overall system's behavior.
The rather simple example of an edge capacitor reveals how important it is that we gain a proper understanding of the real-life characteristics of such planar power systems in order to exploit their advanced capabilities for improving EMC and optimizing power integrity. It also becomes obvious that proper design of such systems is no trivial matter.

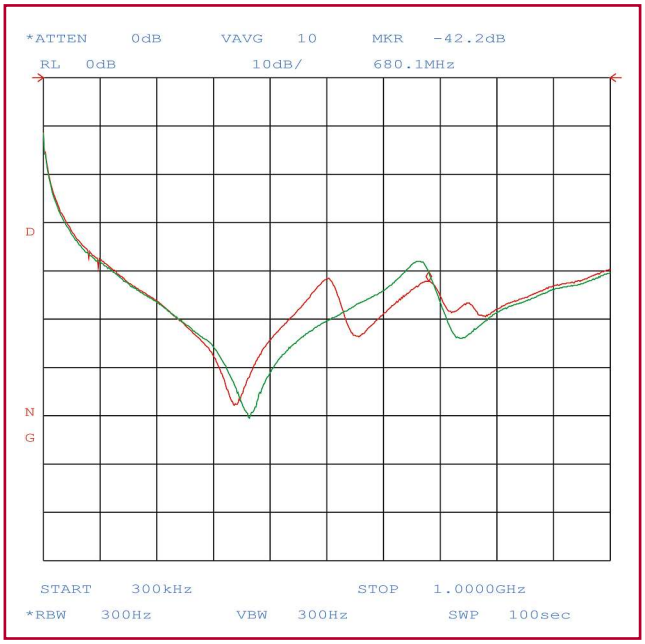


Figure 6:
The measurement shows a value that is proportional to the magnitude of impedance as measured at port CN1 within the meltemi economic board's 1V2 FPGA core power system. It reveals a reduction of the shunt resonance at 675 MHz by about 40%.

In most cases, design engineers will employ an appropriate simulation tool to analyze and optimize the entire power system – a topic covered in chapter 13. *(cm)*

References:

[1] „Die Mär vom Plattenkondensator," Nils Dirks, ELEKTRONIKPRAXIS Sonderheft 2/2005, p. 42ff
[2] „Die optimale Prozessor-Stromversorgung," Prof. Chr. Dirks, Elektronik 23/96, p.134ff
[3] "Reducing Simultaneous Switching Noise and EMI on Ground/ Power Planes by Dissipative Edge Termination," Istvan Novak, 7th Topical Meeting on EPEP 10/98
[4] „Kantenabsorber aus Karbon" (patented, kantenabsorber@emv.biz)

Electromagnetic properties of power systems

Quiet, please!

"Quiet, please!" Those words neatly express designers' needs with regard to the interference levels within the power systems of their printed circuit boards. The proven benefits of wide-band capacitor groups – extended to include precise consideration of the structure characteristics – leads to optimal EMC results combined with excellent system stability. Using the "meltemi economic" board's 1V2 FPGA core power system as an example, EMC expert Nils Dirks explains the characteristic properties of such power systems. Wide-band capacitor groups and selected capacitors will then be added to the bare planes to cope with the deficiencies of these systems and yield low impedance across broad frequency ranges.

by Nils Dirks



In the early 1990's, EMC experts came up with the concept of broadband capacitor groups [1]. However, the need to design power systems that are particularly efficient in terms of performance as well as broadband EMC was not a pressing issue in mainstream electronics back then.

In the recent past, however, designers have been increasingly confronted with two typical problems:

1. The specified levels of tolerable supply voltage break downs at the semiconductor components (RAM, CPU, ASIC, FPGA, etc.) are continuously being reduced. This generates demand for ever lower power system impedances – nowadays in the milliohm realm.
2. Modern digital electronics already consume average operating currents within the multi-ampere range. The resulting (fast) current pulses drawn from the power system reach peak values that rise clearly above the average input current and create substantial EMC problems.

The advantages of correctly designed power plane systems not only solve these two problems, they also provide a multitude of additional advantages. Nevertheless, this article will only be covering the two issues cited here, because they already provide more than sufficient motivation for proper design of these power systems.

We will examine the meltemi economic board's 1V2 FPGA core power system in order to show the electromagnetic properties of the bare plane system and develop a concept for dealing with the deficiencies observed. The schematic layout of the power/GND plane is depicted in figure 1. The green trace in figure 2 shows the magnitude of the impedance measured at test port CN1 (Pos 35 mm, 24 mm) of the unpopulated meltemi economic board V.1.0. A properly installed SMA connector provides RF-proof access to the power plane system, thus enabling accurate (network analyzer) measurements. The details of a suitable measurement setup and/or measuring procedure greatly impact the accuracy of the measurement and will be the subject of a later paper.

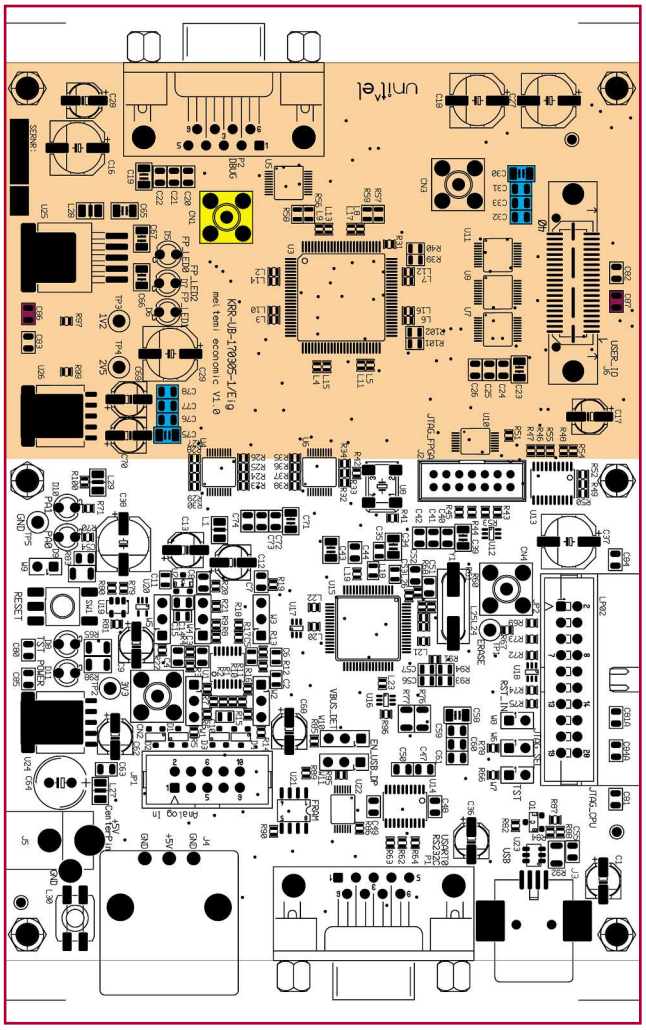


Figure 1:
Rectangular 1V2 FPGA core power system: SMA connector and capacitors

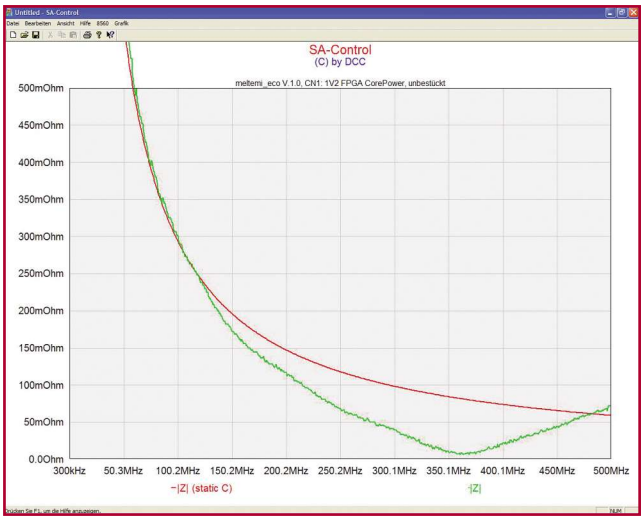


Figure 2:
Magnitude of impedance of the unpopulated 1V2 plane system compared to an ideal capacitor

At low frequencies, the measurement very clearly shows the capacitive behavior of the structure consisting of a power and GND plane and a 50-µm thick FR4 dielectric between them. In comparison, the red curve represents the impedance of an ideal capacitor of 5.5 nF, which corresponds exactly to the capacitance of the unpopulated power system measured at a frequency of a few kHz.
Up to a frequency of approx. 130 MHz, the two curves run practically congruently. Our power system apparently behaves like an ideal, lumped capacitor (no parasitic components, no spatial extent, etc.). At higher frequencies, the ideal capacitor exhibits a continuous decrease in impedance, while the power system shows an extreme minimum impedance at approx. 360 MHz and assumes inductive behavior towards higher frequencies!

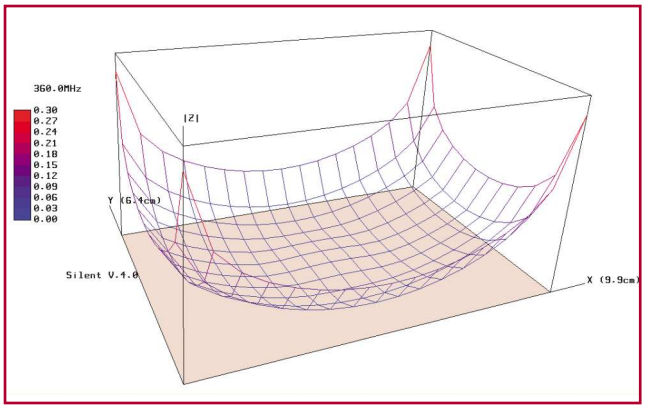
The impedance is not only a function of frequency but also of the test port's position

The causes for this have already been explained in detail in [2] and should be well understood. At first glance, one could argue that the model of the ideal capacitor was still usable up to frequencies of around 500 MHz, because the impedance values that were actually measured are obviously lower (better) than those of the ideal capacitor. Here, we might remind the reader that the observed impedance in such distributed (non-lumped) power systems is not only a function of the frequency, but also of the test port's position! Measurement at a frequency of 360 MHz determines an impedance of approximately 10 mΩ at the location of test port CN1. By means of simulation, the magnitude of impedance at all positions of the system can be made visible for the frequency in question (figure 3).
As with the measurement, the simulation also shows impedance barely below 10 mΩ at the position of test port CN1. Much more obvious, however, is the fact that at other positions (such as the corners, for example) completely different conditions prevail: Here, observed impedances are some thirty-fold higher than the values found at the center of the plane system, which makes the necessity of evaluating the distributed properties of these systems obvious.
Thanks to the meltemi economic board's very well designed power systems, the values reached at the corners of this system are still within an acceptable range. Strict adherence to basic design requirements (such as the use of continuous planes without cutouts, avoidance of narrow sections, use of very thin dielectrics, etc.) is a mandatory prerequisite in this case. Failure to abide by these rules almost always results in much higher values occurring at various positions within the plane system and leads to a multitude of EMC/EMI problems.
In order to avoid such problems, today's simulation tools employ much more complex and accurate models for the characterization of power plane systems, with the classic field solver being only one well-known option. With the aid of an appropriate software tool, potential problems in a given power system can be identified early on in the design phase, thus enabling design engineers to successfully resolve these issues by implementing the required counter-measures.
Once we know the real-life properties of such planes, a multi-step approach is quite useful for ensuring low impedance across the various frequency ranges:
One major step is the design of a broadband capacitor group [3] to maintain low impedance at frequencies for which the plane system does not yet provide sufficiently low values. The

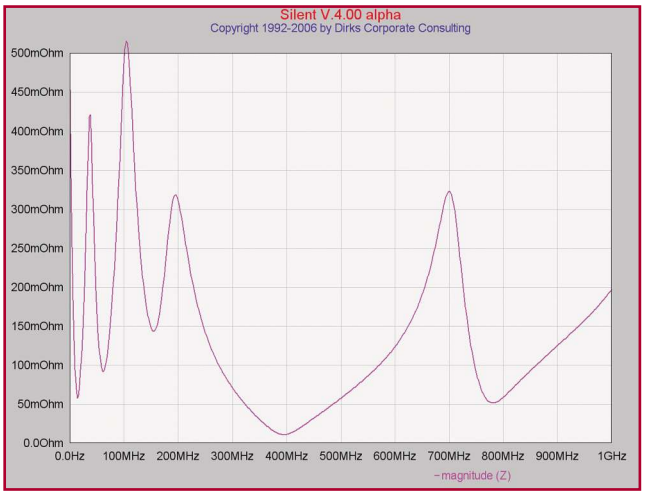
resulting impedance profile as determined by means of simulation/optimization can be seen in figure 4. The voltage regulator and bulk decoupling ensure low impedance at very low frequencies (up to a few MHz) – another design step that will not be shown in detail here. At higher frequencies of up to approximately 300 MHz, the broadband capacitor group (100nF 1206, 10nF 0805, 2.2nF 0805) reveals the typical resonances while maintaining low values overall across the entire range.
Designing the capacitor group to optimally complement the characteristics of the particular plane system ensures a low-impedance hand-over towards higher frequencies. The properly designed plane system itself will then maintain low impedance values towards higher frequencies as long as no resonances are encountered. The 1V2 power system shows initial resonance around 700 MHz, which is caused by standing waves within the distributed plane system. Thanks to the well-planned layer stack-up and favorable plane outline, this resonance reveals a peak value around 300 mΩ and it will not usually require further treatment.
The extent of the agreement between the measurement results (figure 5) and the simulation data is astonishing: The simulation has not only precisely predicted the capacitor group's resonance behavior; it has also correctly depicted the structure characteristics. The slight disagreement in resonance frequencies suggests that the dielectric constant for the test-board dielectric differed slightly from what was assumed for the simulation. Because the phase velocity strongly depends on the dielectric constant, so do the frequencies at which resonances are observed.

The "maximum display" can make things significantly easier

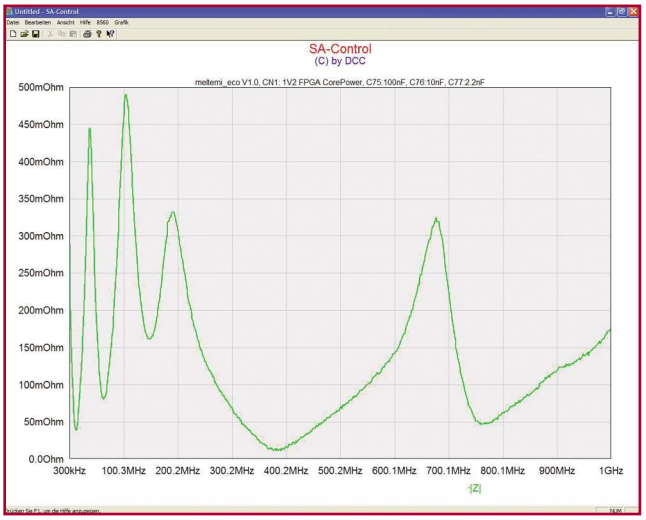
Up to 1 GHz, the measured impedance remains clearly below 1 Ω, which is excellent news, especially when we consider that these are the results at the position of test port CN1! But what about the remainder of the system?
The measurement only shows a "single page of the book". The remaining pages are the impedance curves to be observed at all the other positions within the plane system. Due to the excellent agreement between the measurement and simulation results for the test-port position, we can rely exclusively on the use of simulation for the remaining positions, which saves us a lot of soldering.
Nevertheless, even examination by means of simulation could become somewhat more complex, because we need to take into account one impedance curve (see also figure 3) per location. To judge the system's broadband performance, one would need to mentally combine all these curves, memorizing all the positions and frequencies at which the impedance limit is busted. When it comes to gaining an immediate overview, the "maximum display" can make things significantly easier. This type of diagram (figure 6) provides a sort "worst-case" evaluation by displaying the maximum impedance value found for a particular position throughout the entire frequency range. These maximum values are then displayed as a spatial distribution, and can thus be directly correlated to the location in the plane system. The maximum value found on the scale is 1.66 Ω. Looking at the spatial distribution, this maximum value is found in the upper left corner of the plane system. It states that – within the frequency range analyzed – no impedance greater than 1.66 Ω will be encountered here. When we examine the actual spatial distribution of the impedance at the discrete frequencies (not shown), we find that this particular peak is caused by a cavity ►



■ Figure 3:
Magnitude of impedance for all locations of the 1V2 system at 360 MHz



■ Figure 4:
Magnitude of impedance (simulated) of the plane system with a capacitor group at test port CN1



■ Figure 5:
Magnitude of impedance (measured) of the plane system with a capacitor group at test port CN1

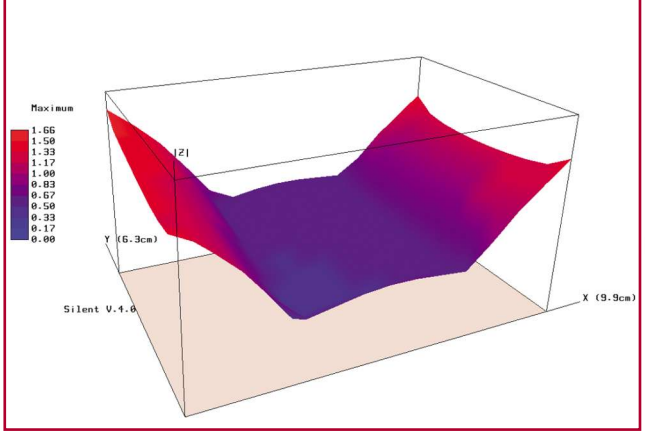


Figure 6:
Maximum magnitude of impedance for all positions of the plane system up to 1000 MHz

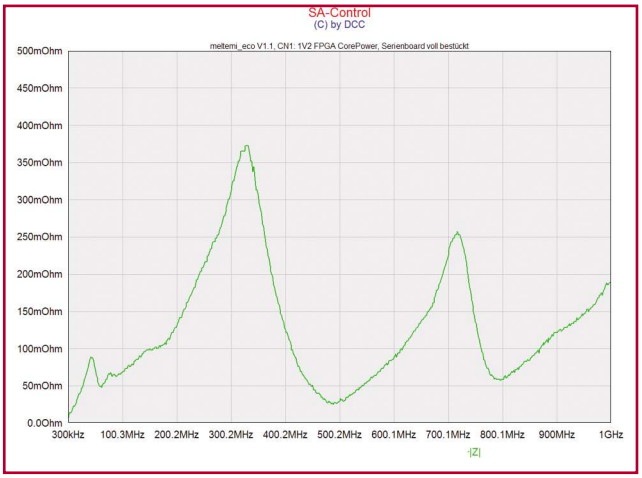


Figure 7:
Measured magnitude of impedance: populated board

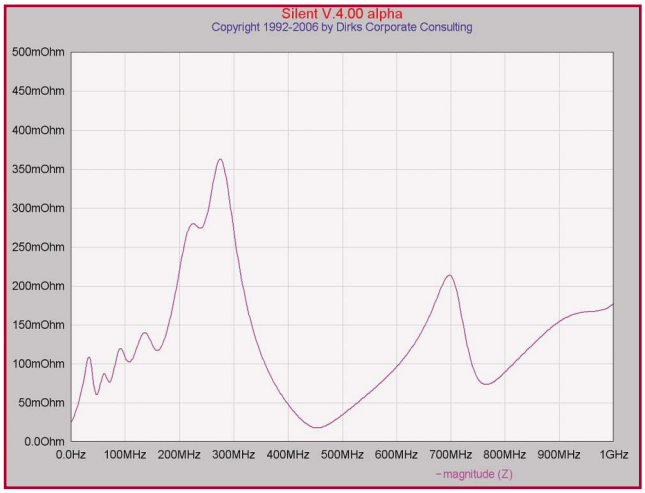
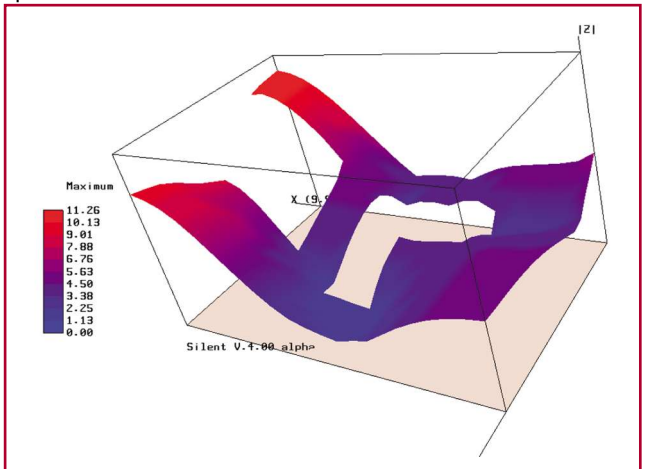


Figure 8:
Simulated magnitude of impedance: populated board

Figure 9:
Maximum |Z| for all positions of an inhomogeneous plane system up to 1000 MHz



Chapter 13

resonance at a frequency of 700 MHz. At this very frequency, the observation at test port CN1 (see figure 5) only showed a value of 0.3 Ω, which hid the resonance's true magnitude.
The worst-case values shown for major parts around the center of the planes lie fairly evenly in the 0.5 Ω range; in the proximity of the short edges, however, rising values up to approximately 1.6 Ω are to be found.
The installation of an additional capacitor group at the position (81 mm, 21 mm), as well as edge-capacitors [4] at the system's short edges, are then used to further improve the situation. Consequently, the power system's very low impedance region (roughly the blue portions in figure 6) expands and shows even smaller values (< 0.3 Ω), while the maximum values at the corners are cut by 25%.

Characteristics of such power systems can be predicted using suitable simulation tools

The concept outlined above using an otherwise unpopulated board has been applied to all the meltemi economic board's power systems. To prove the applicability of the concept for real-life PCBs, a measurement has been made using a fully populated, operational board and then compared to the simulation (figures 7 and 8). Here we see very good agreement, although quantitative deviations are present within some ranges: In the frequency range up to ~200 MHz, the simulation obviously assumed capacitor losses lower than those encountered in the measurement, which results in real-life impedance being some 40 mΩ lower (better) than predicted. The first resonance peak, which results from the interaction between the already inductive capacitor group and the capacitive impedance of the plane system, is precisely predicted in terms of amplitude, while the prediction of the peak frequency is somewhat too low. This deviation is due to the accuracy constraints of the underlying models, as well as to tolerances, and it does not pose a problem in practical applications.
Thus, we can say that the electromagnetic characteristics of such laminar power systems including capacitors can be predicted and optimized very well using suitable simulation tools. The ability to identify and mitigate unwanted resonances is an important prerequisite for designing reliable power systems with favorable EMC characteristics.
The effects shown in this paper can scale into very troublesome ranges if the geometry of the power systems is less favorable, which results in EMC/EMI problems and stability issues that could be very difficult to trace. Figure 9 shows the spatial distribution of the maximum impedance for a power system (120-µm dielectric) of rather inhomogeneous shape. Omitting additional measures to control the various modes in such systems would definitely cause trouble!
The simulations shown were accomplished using Silent V.4.0.

References:

[1] "Breitbandentkopplung von Versorgungsspannungen auf Leiterplatten," by Prof. Chr. Dirks, Dipl.-Ing. U. Margieh, Elektronik 20/1992, p. 97ff
[2] "Die Mär vom Plattenkondensator," Nils Dirks, ELEKTRONIK-PRAXIS Sonderheft 2/2005, p. 42ff
[3] "Die optimale Prozessor-Stromversorgung," Prof. Chr. Dirks, Elektronik 23/1996, p.134ff
[4] "Der Kantenkondensator," Nils Dirks, ELEKTRONIKPRAXIS Sonderausgabe „Die Leiterplatte 2010", April 2007

Example of application – fast signal processing

Operations with high Resolution Motion Pictures

The last contributions focused on the hardware development of the "meltemi" platform. One possible area of application for the meltemi board is real time image processing. This contribution addresses a fundamental image processing model as well as aspects of data transfer bandwidth. Here, specially questions of the primary data transport between image source (e.g. scanner or camera) and a motion image data processing system for high special resolution will be covered. The contribution will also address basic operators within an image processing system.

by Helmut Keller



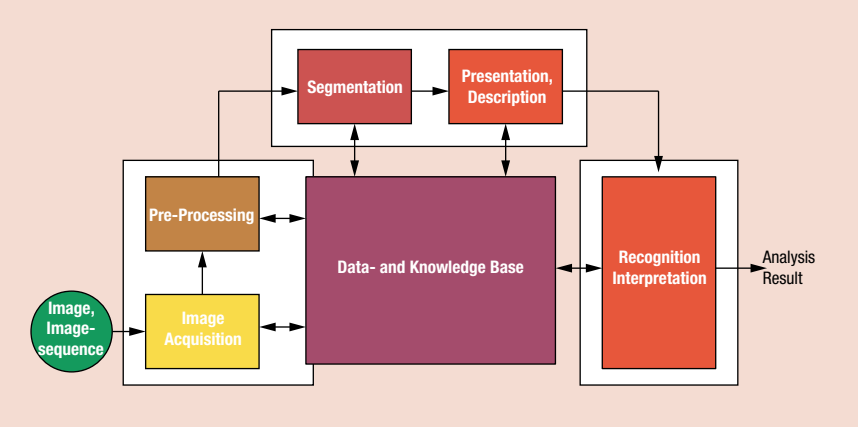


Figure 1:
Model of significant possible signal processing domains within an autonomous image processing- and analysis system

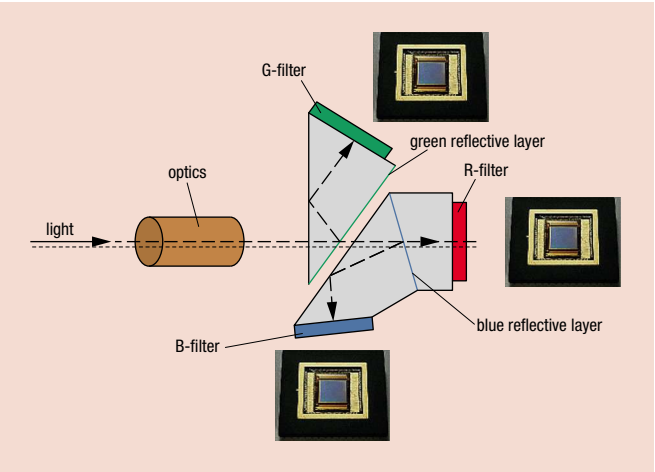


Figure 2:
Three-chip RGB camera system with a prism-beamsplitter used as R/G/B bandpass filter

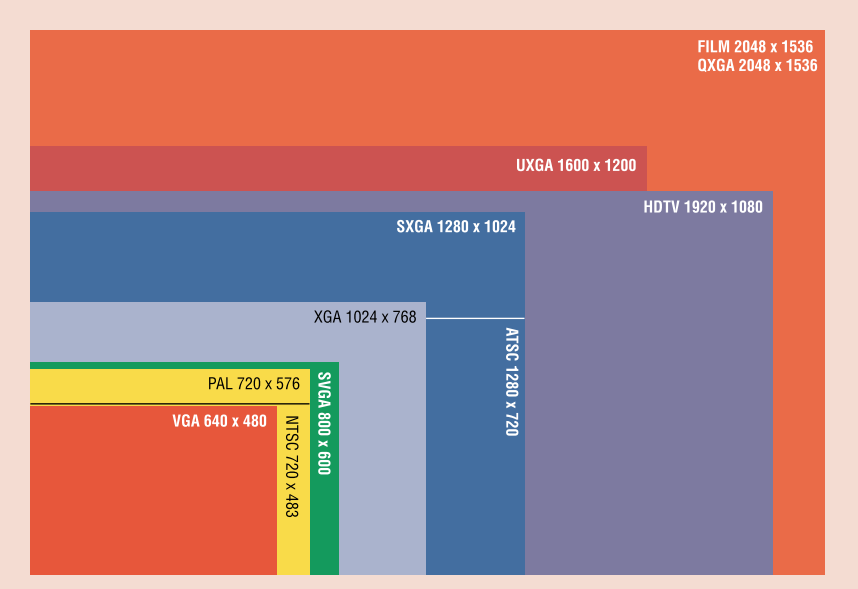


Figure 3 shows a summary of important image formats between VGA, the SD video formats PAL and NTSC via HDTV up to QXGA, which also corresponds to the 2k DigitalCinema format named after the 2kpels per line. Within formats of high spatial resolution, the 4k format grows more and more important as "Digital Intermediate" in the DCinema production chain. There are discussions about an 8k format.

Due to their construction, FPGAs suite very well in signal processing application, specially image processing. With these devices real time processing of big image formats, as they are used with HDTV and digital cinema, becomes feasible.
Signal processing operations within the area of image processing comprehend processes as e.g. image acquisition via image acquisition systems (cameras, scanners), image format conversion and preprocessing. Also involved could be processes as e.g. image segmentation, mixing of images, insertion of sub images (keying), image filtering and colour correction.
With „big" image formats with high spatial resolution considerable volumes of data are involved. Often one has to use data compression. With data compression, the volume of the information to be transported and processed is reduced without degrading the image.
Generally, image processing operations, which in their practical applications are used in a bundled form, can be analysed and compared quite well by looking at them separately using reference models. Based on the image processing model according to Gonzales/Woods [2], some of the important image processing operations, which can be realised with embedded methods using signal processors and FPGAs shall be detailed here.

The image processing model

The model presented in figure 1 shows some of the possible important processes within image processing, which together could lead to an automated image processing and -analysis system.

Image acquisition

In the case of image acquisition, image information from an image source (e.g. line scanner, camera or image storage device) is imported and processed in a form, that this information is suitable for further processing within the image processing unit.
Image storage and image transmission systems often use the 4:2:2 component format, with which for each pixel one luminance (Y) value is transmitted but in contrast alternately only one blue or one red colour difference signal.
Within an image processing system, in many cases the representation of luminance and chrominance signals in their full spatial resolution (4:4:4)s necessary. This adaption to the given pixel raster can be performed within the block "image acquisition" through adequate interpolation processes.

In the block "pre processing" in the case of grey scale images the adequate preparational operation on the source image is performed through processes as e.g. grey scale stretching or transformation of the grey scale characteristics, [6].

Color images

In the case of colour image processing, one can, technically speaking, assume, that out eyes on one hand only detect optical images only from a small part of the physical colour spectrum, namely between infrared and ultra violet (about 800 to 400 nm), on the other hand these optical images these optical images are only sort of a "false colour representation". Based on economic and physiological factors, the transmission of the visual colour information within 3 technical colour channels (RGB) has proven to be sufficient. Each of these colour channels represents a bandwidth of about 150 nm from the physical spectrum. Besides this 3 colour wavelength multiplexing approach a more detailed division (e.g. into 7 channels) would also be possible. There exist enhanced resolution solutions for special applications. With many broadcast- and consumer applications (still- and motion picture, TV, video and DCinema) the RGB – representation or derived formats as e.g. the component representation (VUV respectively. YcrCb) are established. Figure 2 shows a typical 3 chip RGB camera system with a prism-based beamsplitter, which is applied as RGB bandpass filter.

Spatial resolution with images and image formats

A major issue with the design of image processing operators is the basic spatial resolution of the images to be processed. Concerning image formats, the characterisation of resolution can be performed by providing the number of horizontal and vertical Pels involved. Figure 3 shows a summary of important image formats between VGA, the SD Video formats PAL and NTSC via HDTV up to QXGA. The latter conforms also with the 2k DCinema format, termed after the involved 2kPels per image line. Within the range of formats with high spatial resolution also the 4k format is starting to become relevant as "digital intermediate" for digital cinema applications. An 8k format is being discussed.

An example for an image sensor with high spatial resolution shall be given here too: The 4 Mpixel CMOS image sensor PB-MV40 [7], figure 4.

For every column of the 2352 image sensor columns one dedicated A/D converter is provided, the analog transport of intensity information across an image line, as it is performed within CCDs, is eliminated here.

Primary data rates with different formats and image resolutions

First, the total image pixel count of one image frame of the formats shown in figure 3 shall be considered.

CCD and CMOS Image Sensors

With today's image sensors, on distinguishes between sensors based on the charge coupled image transport devices (CCDs) and CMOS devices. With both devices, at a given special resolution the transformation from an optical into an electrical signal is performed in a similar way. In the active sensor areas of an image sensor with a given special resolution, the light intensity at each PEL-location is transformed into a proportional electrical charge utilising the photo-electric effect.

CCD- and CMOS sensors differ in the way, in which the now available "electrical" image is transported. While CCDs use a charge transport mechanism with analogue shift registers, the A/D conversion being located typically at a place located after the analogue line shifting mechanism, CMOS sensors realise the A/D conversion without this analogue transport of the intensity information near the pixel area and in parallel. The bottleneck with CMOS sensors is, how to get out the digital data from the device in parallel.

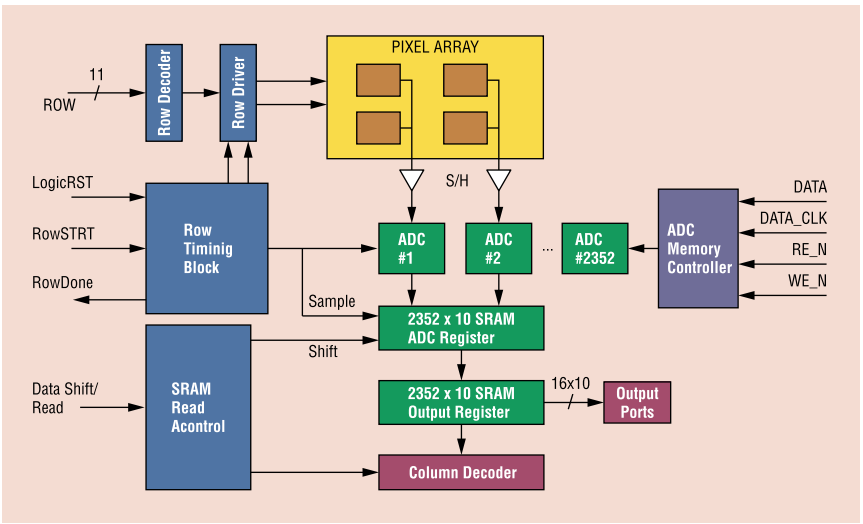


Figure 4:
General view of the 4-Mpixel-CMOS-sensor PB-MV40: an example for an image sensor with high spatial resolution

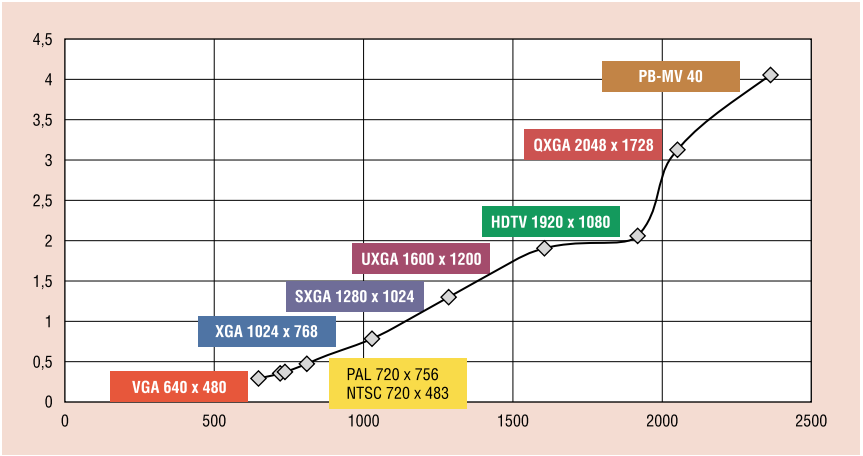


Figure 5:
Total pixel count M for an image sensor [Mpels] as a function of the number of pels/line depending from the associated format. With 4:3 image ratios: M[Mpels] = (pels/line)2 · 3/4

The diagram in figure 5 shows the total frame pixel count of the discussed formats as a function of the associated pixels per image line.
The majority of the formats (VGA, SVGA, XGA, UYGA and QXGA) show a ratio of 4:3 between the number of pels per line and lines per image, the 16:9 formats (ATSC and HDTV) are, besides the SDTV formats, SXGA an the 4 Mpel image sensor, main reasons for a deviation from the 4:3 image ratio slope in the diagram.
From the diagram the significant number of discrete display- or sensor-pel locations can be depicted for lager image formats.
With 3 chip cameras (true RGB image sensors) the number of the image sensing elements from figure 5 has to be multiplied by 3. So in the case of camera with the 4 Mpel image sensor this results in 12M sensing elements or pels. Beyond the 4 Mpel sensor size the local registration of the 3 colour planes becomes problematic and alternative approaches have to be considered in contrast to the now mainly used RGB camera system with its prism beam splitter.

Primary data rates

The volume of data to be transported per second from an RGB Image sensor system to the functional module "image acquisition" can be depicted from figure 6. A bit-resolution of B = 10 is assumed for each intensity channel. (Sometimes, within DCinema or broadcast applications, bit resolutions of B = 12 or 14 are often realised).
At 24 frames/s progressive scan (Digital-Cinema, P24), when PB-MV40 sensors with a bit resolution of B = 10 are used, this results in a primary data rate of nearly 3 Gbit/s for an RGB sensor system. The mentioned sensor is able to support frame rates of up to 240 f/s with full spatial resolution.
With such a high speed camera system (e.g. for high frame rate applications and special effects) the image source produces a data volume of nearly 30 Gbit/s, which reliably has to be transported from the interface of the image sensors (in case of the PB-MV40: 3*16 = 48 10 bit ports) to the "image acquisition" subsystem and from there to the "preprocessing" sub-system. *(cm)*

Image format	Size			Frames	Data rate
	H-Pixel	V-Pixel	M-Pixel	fs	Mbit/s
VGA	640	480	0,31	25	230
NTSC	720	483	0,35	30	313
PAL	720	576	0,41	25	311
SVGA	800	600	0,48	25	360
XGA	1024	768	0,79	25	590
SXGA	1280	1024	1,31	25	983
UXGA	1600	1200	1,92	25	1440
HDTV	1920	1080	2,07	25	1555
FILM	2048	1536	3,15	24	2265
PB-MV40	2352	1728	4,06	24	2926
PB-MV40	2352	1728	4,06	240	29263

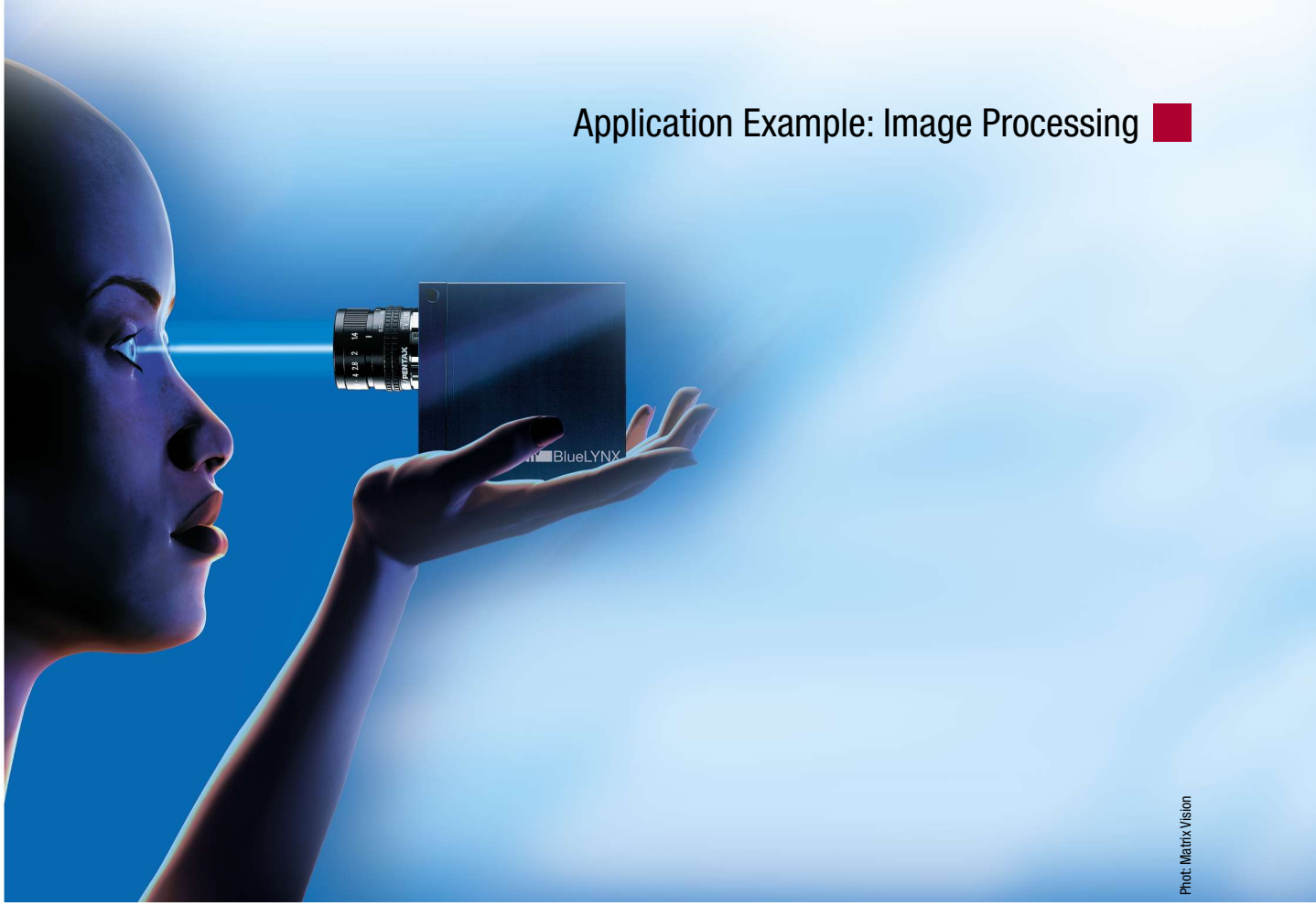
Figure 6: Primary RGB data rates at different spatial image formats and progressive scan frame rates between 24 and 30 f/s

Literature and References:

[1] Digital Signal Processing, A.V. Oppenheim, R.W. Schäfer
[2] Digital Image Processing, R.C. Gonzales, R.E. Woods
[3] Fundamentals of Digital Image Processing,A.K. Jain
[4] Operatoren für die Bildverarbeitung, R. Klette, P. Zamperoni
[5] The Art of Digital Video, John Watkinson
[6] Zweidimensionale Signalverarbeitung mit FPGAs, H. Keller, p. 59ff. ELEKTRONIKPRAXIS, Special Edition 11/2003
[7] PB-MV40 : 4-Megapixel-CMOS-Active-Pixel
[8] Digital Image Sensor; Micron

Operators in "Image Acquisition": change in spatial resolution

The domain „Image Acquisiton" handles the necessary processing and possible conversion steps from the optical image via the analogue electrical image, which is spatially – quantized according the sensor pixel resolution, up to the digital image, which is the amplitude – quantized numerical version of the analogue electrical image. In many cases, CMOS- or CCD image sensors today realise these processing steps.
Spatial quantisation is the result of the position of the individual image sensor elements on the sensor chip. In many cases with CCD sensors, always with CMOS sensors, the A/D conversion is realised directly on the chip and what remains, is the transport of the primary raw image data with the necessary transport bandwidth.
If the video signal source is analogue, the A/D conversion has to be performed in the domain "image acquisition". Finally it is necessary to present the primary information (the "digital" image) in a spatial resolution, which is compatible with the next processing steps.
In that sense there may be also operators included in the domain „image acquisition", which are able to modify the spatial representation of the digital image in order to be compliant with the image processor (e.g. the hardware mapping within the image RAM address generator) and to operators within the image processor, which normally have to be sourced with images of a certain format. Some of these operators are described in [8]. These operators implement the sampling theorem with spatial signals (with scan-lines: s(x), with rectangular source images and with image sensors: s(x,y)).
Basically it is possible, to increase images in their spatial resolution by applying the interpolation factor i. The interpolation factor shall be considered to be an integer here.
To create an HDTV line from a VGA image line (640 pels), the interpolation factor 3 has to be applied. The VGA image is, simply spoken, expanded to the 3-fold line length of the HDTV horizontal raster by inserting 2 interpolated filling Pels between two formerly neighbouring VGA pels.
Besides linear interpolation techniques, which can be realised fairly easily, spline- or sinx/x interpolation together with special interpolation filters can be applied, providing more acceptable visual results for the interpolated and, in its spatial representation enlarged image
The reverse operation – the reduction of spatial resolution – can be reached though decimation of the spatial signal with the decimation factor d (here d is also considered to be an integer).
One can convert an HDTV line to fit on a VGA display by implementing the decimation factor d = 3. In the most simple case, after the first HDTV pel the next 2 pels are dumped, the 4th HDTV pel stays alive and becomes the 2nd VGA pel in the VGA line, etc. If non-integer – interpolation or – decimation processes are needed, one can apply a combination of an integer interpolation- and decimation process.



Phot: Matrix Vision

Real-Time processing of complex image formats

FPGAs in two dimensional Signal Processing

Due to their structure FPGAs are perfectly suited to solve tasks in two dimensional signal processing, e.g. in the area of image processing. Nowadays fast implementations of processes like colour space correction, contour detection and image compression are required in this field.

by Helmut Keller

In recent years FPGAs have been realised, which offer resources for massive parallelized solutions in vectorisable tasks. This instance probably leads to tremendous increase in speed acceleration of vectorisable processes as compared to conventional scalar processes An adequate provision of I/O bandwidth results in a significant increase in data throughput compared to today's workstation solutions.(With an adequate provision of I/O bandwidth a significant increase in data throughput as compared to today's workstation solutions can be achieved).

By means of this development also the realtime processing of complex image formats, required e.g. for HDTV or digital cinema, starts to become applicable and economically feasible in more broadening areas or even consumer electronics.

The following three examples discuss the advantages of FPGAs in image processing when operatorsby making use of operators.

First one simple case of interpolation will be discussed, a process applicable used e.g. for the conversion from small to big display formats. The second example is about a simple case of colour transformation. Example 3 deals with the Discrete Cosine Transformation (DCT), which is used in many areas of image data compression.

In all these cases transformations‚in space' will be considered, making use of 2-D transformation operators.

As these operators can also be realised in parallel (the limit of parallel implementation is determined by the resources of the FPGA considered) and as these operators can be executed massively and independently in parallel, the term 'processing in space' can be applied more preci- ▶

Application Example: Image Processing

Figure 1



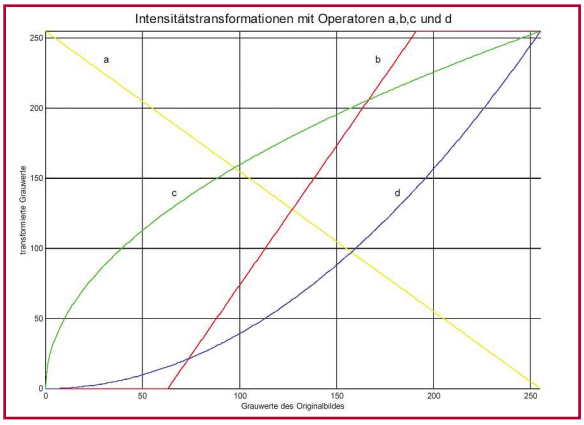


Figure 2

sely of processing in the 2-D space or in the area limited by the silicon die on which the FPGA physically is implemented). In contrast to scalar processors, whose speed is mainly dependent on the clock frequency, in the field of the vector processes currently discussed acceleration factors become visible (apparent) which are proportional to the number of operators realised (applied on?) on an FPGA silicon die. The acceleration factor increments (theoretically, and considering a certain FPGA technology) with the square of the side length of the FPGA chip.

Example 1:
Conversion of display formats of digital images

Considering image processing, an image can be seen as a two dimensional distribution of intensity values. Such an image normally is captured by a certain recording equipment, e.g. a CCD camera, where the CCD image converter is positioned in the image plane of an optical camera device at a place, where also photographic film can be located. The term 'digital image' is used for the description of images, where the local distribution of the intensity information (given through the positions and distribution of CCD Image sensing elements) as well as the intensity information itself (given through the bitresolution B of the CCD-A/D converter) are discrete. Two fundamental problems of 2-D signal processing:

Pixel decimation and pixel interpolation. For our example a CCD bit resolution B = 8 shall be considered (480 × 640 × 256-image). With the conversion of a digital image into another pixel format two fundamental problems of 2-D signal processing become apparent: pixel decimation and pixel interpolation. While the conversion of a 480 lines times 680 columns image into an image with 240 lines and 320 columns can be achieved through elimination of even lines and columns in its simplest form, expansion of the source image into the format 960 × 1280 × 256 has to make use of an interpolation process. In the latter case, the grey values for the new pixel elements (PELs) to be introduced during the interpolation process will be calculated out of the grey values of the neighbouring already existing PELs. Here either linear interpolation (calculation of the mean value of neighbouring PELs) can be used or preferably a more advanced interpolation algorithm.

One elementary advantage if operators are used

The interpolation example highlights already one elementary advantage if operators are used. Through fast input channels bigger image constituents can be read in (e.g. one or several image lines of the image to be expanded in our sample case). The simple interpolation-operation originally is PEL-specific, considering only 1 PEL together with its immediate neighbours. Now this operation can be performed on a certain part of the image 'as a whole', i.e. on several or many PELs in parallel, using several or many interpolation operators, realised in the silicon of the FPGA-die in parallel. Through fast output channels the newly formed image constituents with enhanced resolution can be transported to an image destination, e.g. to a projection system.

Example 2:
Colour and intensity transformations

Colour is a powerful description attribute and in many cases it can facilitate the identification of objects or their extractions from a scene. Image processing by the human visual system reveals a seperability of only about 24 gray levels in contrast to several thousands of colour tones. The scope of colour processing roughly can be divided into the areas of error- or false colour processing, in contrast to full colour processing, the latter originally being dedicated mainly to professional application areas. By the introduction of CCDs and CMOS image converters down to the consumer level, full colour processing and associated colour models as e.g. RGB, CMY, YIQ, HIS or HSV are common in many fields today.

In this context, for the reason of simplicity the big area of image colour transformations shall be limited to grey value images only. These images are provided by B&W cameras or as single colour output from an RGB signal. Intensity transformations represent an important tool in the area of image enhancement. Besides subtractive methods, averaging, histogram processing and linear as well as nonlinear filtering with convolutions masks, the intensity transformation represents an image processing method in space (in contrast to methods in frequency).

Members of this class of operations appear in the form g(x,y) = T(f(x,y)), where f(x,y) represents the source image and g(x,y) represents the processed image; T is the transformation-operator on f, defined in a certain environment of (x,y). Intensity transformations can be categorised into grey value transformations, the bitplane decomposition and others. Examples of grey value transformations are e.g. PEL operations with operators for amplitude scaling, for the expansion of the grey scale, for the transformation of the grey scale characteristics or for the equalization of the grey value histogram. Starting point for some intensity transformation examples shall be the following 8 bit source image (figure 1).

Figure 2 shows some transformation characteristics for the transform operators (a)

inversion, (b) grey scale expansion within the range of 25% to 75% of the source image grey scale and the grey value transformation according to the exponential function [5]

$$s_i(x,y) = s_{\max}\left(\frac{f(x,y)}{s_{\max}}\right)^{r_i};$$

with the exponents (c) r = 0.5 and (d) r = 2 (figure 2).
The application of the operators (a) to (d) deliver the following resulting images:
(a) inversion (figure 3)
(b) grey scale expansion within the range of 25% to 75% (figure 4)
(c) grey value transformation according to the exponential function r = 0.5 (figure 5)
(d) grey value transformation according to the exponential function r = 2 (figure 6)

Example 3:
Discrete Cosine Transform (DCT)

As a final example the DCT shall be discussed, a transformation applied widely in the area of image data reduction. This type of transformation is also used with the popular MP3 compression in its 1 dimensional form. In its 2 dimensional form it is applied in still- and moving image compression as e.g. with JPEG [4] and with MPEG. With JPEG, the DCT represents the first step in the compression chain.
Usually a DCT transformation kernel is applied to 8 × 8 PEL elements, the image is compressed by subsequent processing of 8 × 8 PEL image blocks, where the applied transformation kernel has to conform to the results of the JPEG reference transformation according to [4].

$$S(v,u) = \frac{C(v)}{2}\cdot\frac{C(u)}{2}\sum_{y=0}^{7}\sum_{x=0}^{7}s(y,x)$$
$$\cdot\cos\left((2x+1)\frac{u\pi}{16}\right)\cdot\cos\left((2y+1)\frac{v\pi}{16}\right)$$

In the same way the kernel for the reverse DCT transformation has to conform to :

$$s(y,x) = \cdot\sum_{v=0}^{7}\frac{C(v)}{2}\sum_{u=0}^{7}\frac{C(u)}{2}S(v,u)$$
$$\cdot\cos\left((2x+1)\frac{u\pi}{16}\right)\cdot\cos\left((2y+1)\frac{v\pi}{16}\right)$$

$$C(u) = \frac{1}{\sqrt{2}} @ u = 0$$
$$C(u) = 1....@u > 0$$
$$C(v) = \frac{1}{\sqrt{2}} @ v = 0$$
$$C(v) = 1....@v > 0$$
$$s(y,x) = 2D\_Sample$$
$$S(v,u) = 2D\_DCT\_Koeffizient$$

Implemented in a scalar processor, the application of the transformation- and the reverse transformation kernels on a 8 × 8 image data block represents a significant workload, due to the significant number of additive and multiplicative operations to be executed. This results in a significantly high transformation time when applied to multimedia content. Through the implementations of one or more DCT transformation kernels in an FPGA as vector kernel(s) one or more 8 × 8 image segments can be transformed 'as a whole' and maybe in parallel, thereby drastically accelerating processing speeds with broadcast and production image formats. By these means real-time processing is possible even in the latter more sophisticated (demanding) application areas.
Compared to scalar-processors the use of reconfigurable FPGAs in correlation with a suitable microprocessor fulfills the potential of realising pixel operations within a few clock periods. Some of these operations can be designed and realised as operators and they can be specifically optimised for dedicated FPGAs. Additionally these operations can be laid out massively in parallel to support a vector process. In this case the operator is applied not only to a single pixel but to a part of the image "as a whole", leading to significant speed-ups, especially concerning realtime image processing.
Beside the very fast I/O-data channels (transferrate several Gbit/s) the UNIFIRE II/CERO board completely comes up to the mentioned requirements. Even though operators of the described kind usually are loaded as a specific "design" into the FPGA and stay there temporarily resident a high flexibility for different tasks is perpetuated in particular due to the combination of microprocessor and reconfigurable FPGA. *(cm)*

References:
[1] Digital Signal Processing, A. V. Oppenheim, R. W. Schafer;
[2] Digital Image Processing, R. C. Gonzales, R.E.Woods;
[3] Fundamentals of Digital Image Processing, A. K. Jain;
[4] JPEG, IS 10918-1, ITU_T T.81
[5] Operatoren für die Bildbearbeitung, R. Klette, P. Zamperoni;

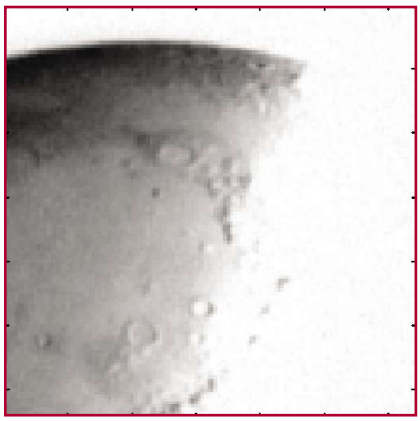

Figure 3


Figure 4

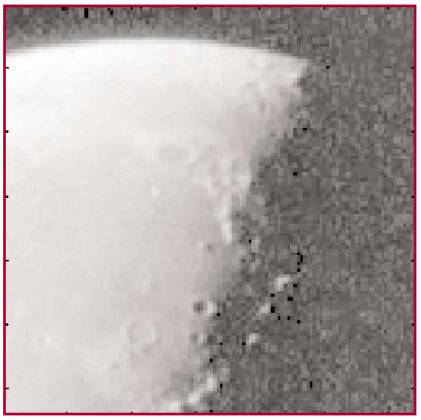

Figure 5


Figure 6

Transmission bandwidth for the years to come

Meet the Challenge

One solution to react to increasing product variety, decreasing product life cycles and faster changes of technology is a developing platform which besides flexibility shows enough transmission bandwidth for the years to come. While some modern semiconductor products already show these abilities with respect to transmission bandwidth on PCB level completely new solutions are to be found in cooperation with the PCB manufacturer and the board assembler. In high speed applications the trial and error approach does not make sense – neither economically nor does it lead to practical results. In a series a consistent solution will be shown by presenting the example of a high speed CPU module.

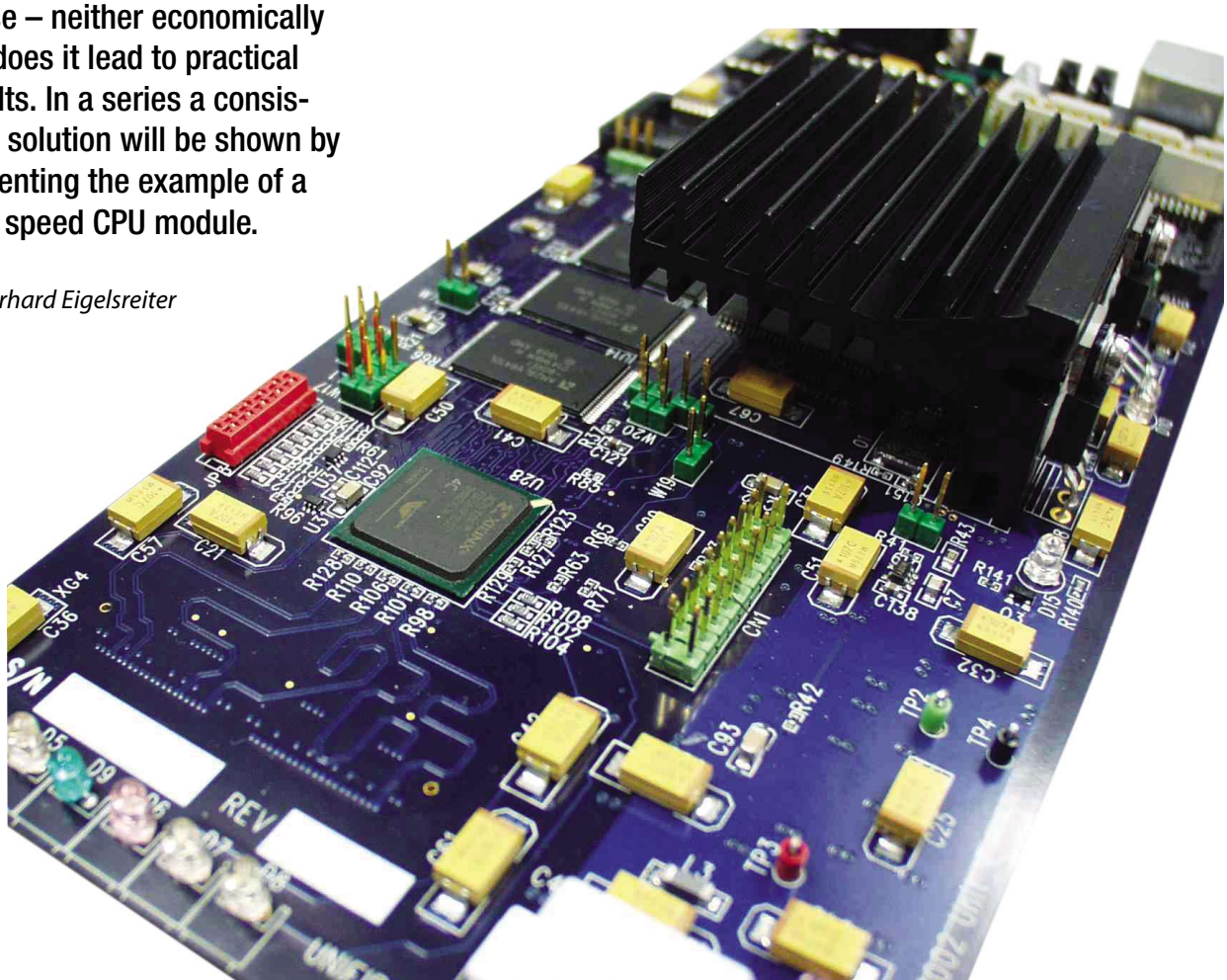
by Gerhard Eigelsreiter

Nowadays demo- and developing boards are built for most efficient hardware useswithout paying much attention to flexible I/O structures. An increasing amount of peripheral devices is being developed by Intellectual Property-(IP-)modules using reprogrammmable logic FPGAs. This reduces free resources available for userspecific solutions. One obvious possibility could be to remove redundant functions on SRAM based FPGAs. Unfortunately unsatisfactory or non existing software tools make the use of these obtained free I/Os impossible in the long term.
The synthesis of multiple serial high speed channels by using complex FPGA structures form the basis for the development and construction of a hardware which will withstand the challenges of the years to come.
By means of the 18-layer board CERO within the UNIFIRE II project we will describe chosen ways to solve the task and the itinerary (path) from the basic idea to the production of the board.

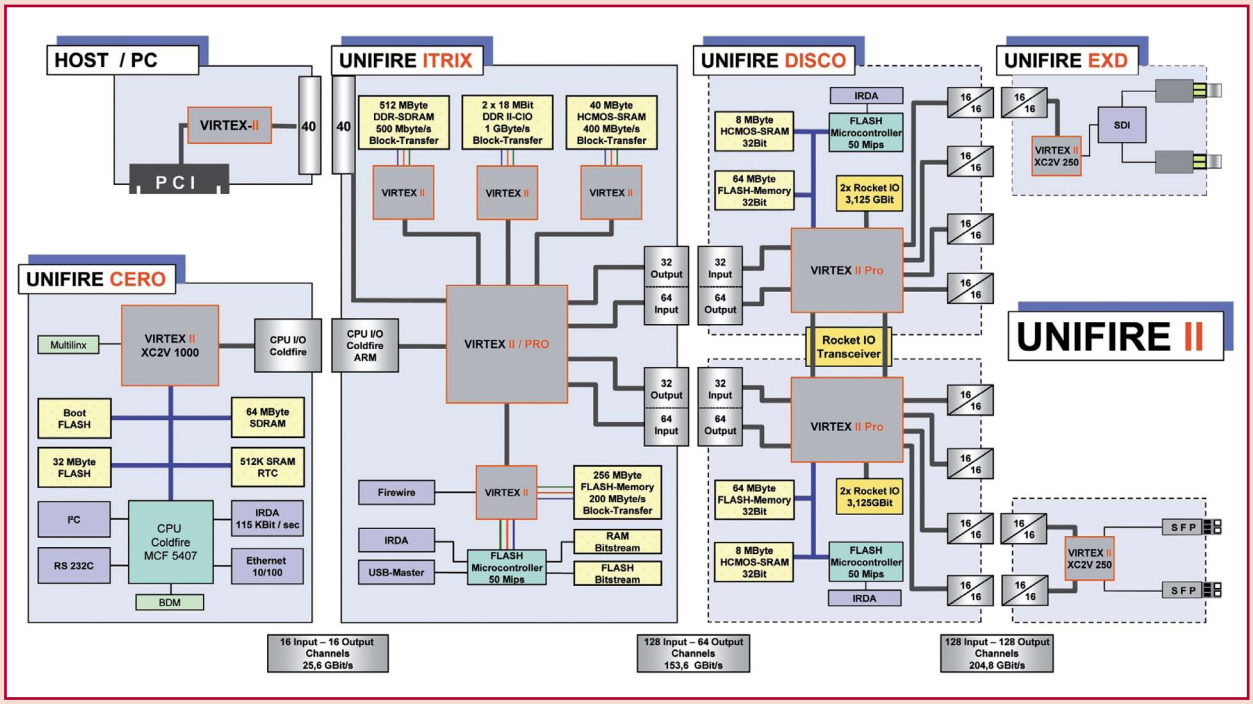
Considerable progress in the development of processor (processing) technologies for chip manufacturing with structures of 0.13µm and below have led to the realisation of ICs with I/O-bandwidths of several hundreds of Gbit/s. SRAM based FPGAs representing the latest (newest) generation of reprogrammable logic provide particularly high flexibility and extended options.

Demand for broadband data transmission

The complexity of these components demands special requirements in the field of the construction of Giga-bit technology hardware. Thus the printed circuit board holds the key position both as a circuit carrier and connecting element. In addition the PCB has to meet the demands for broadband data transmission for the years to come.
To meet these challenges only improving the classical methods will hardly lead to the desired success and conside- ▶



The scalable and reconfigurable high speed platform UNIFIRE II



The scalable and reconfigurable high speed platform UNIFIRE II developed by unit^el is the optimal synthesis of an open development platform on which the application hardware can be immediately implemented. The hardware basis consists of three modules and specific subsystems. The modules, which differ in transmission rates and throughput capacity are constructed to be applicated independently of each other as well. According to their performing capacity and functionality they are assigned to the categories Blueline, Redline, Greenline, Whiteline and Blackline. Optically the modules and subsystems differ by their PCB colour.

The module UNIFIRE II CERO presently uses a Motorola Coldfire CPU. Another module, AERO, using an ARM processor will appear soon. Lower bandwidth interfaces like RS232C, I2C, IRDA and Ethernet for service access, CPU user interface and slow up/download procedures are located on the controller side.
The board is equipped with 64 Mbyte SDRAM, 32 Mbyte FLASH, 512 kbyte SRAM, FLASH BOOT ROM and realtime clock. Presently two operating systems are available: OS9 – a UNIX similar realtime OS-variant for embedded systems and embedded LINUX. The high speed side on the board is equipped with a Virtex II FPGA.

32 LVDS channels are supported which are completely accessible for the user in case of stand alone use of the module. That corresponds to an agglomerate I/O bandwidth of 25.6 Gbit/s.
The CERO module is applicable as a standalone embedded system without restrictions. unit^el offers both the development of subsystems and "spin off" products on customer's request.

The module UNIFIRE II ITRIX (in preparation), category Redline, supports the interfaces FireWire, IRDA and USB master on the "slow" side. This module contains a FLASH controller to load the Virtex II Pro design-elements from bitstream RAM and FLASH devices.
The central Virtex-II Pro FPGA is connected on one side with the CERO or AERO module via LVDS I/O channels.
The other side provides LVDS channel capacity of 102.4 Gbit/s input or 51.2 Gbit/s output or is associated with DISCO building a double module. Taking the CERO LVDS channels into consideration an accumulated I/O bandwidth of 179.3 Gbit/s is resulting. Beyond that 24 bidirectional transceiver channels with an additional bandwidth of 120 Gbit/s max. are available.
As central FPGA the most complex Virtex II PRO P125 with four PowerPC processor blocks can be used as well as two alternate devices. Thus a good balance between needs of system performance and system costs can be achieved. ITRIX is supporting four different memory systems with a total bandwidth of 4.2 Gbit/s all of them working in parallel mode: no buses are existing between the central Virtex II PRO and the memory controllers but exclusively massive parallel LVDS channels with deterministic behaviour are used.

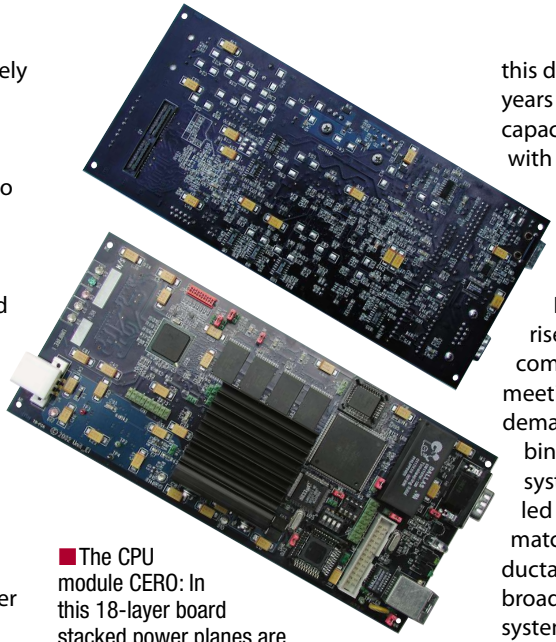
The UNIFIRE II DISCO module, category Greenline, can be used if preprocessing of arriving high speed data streams or post-processing of outgoing data streams is necessary, e.g. data (de-)compression, transcoding, synchronisation, colour space correction and image fusion.
In direction to the EXD-systems, category Whiteline, an accumulated I/O channel bandwidth of approximately 250 Gbit/s could be achieved.

The external interface consists of the modules UNIFIRE EXD and Host/PC. The extremely high bandwidth provided by CERO, ITRIX and/or DISCO is made accessible by small, economically producible submodules for already existing and for future standard interfaces.
Advantage: the core hardware remains independent from any interface standardisation chaos.

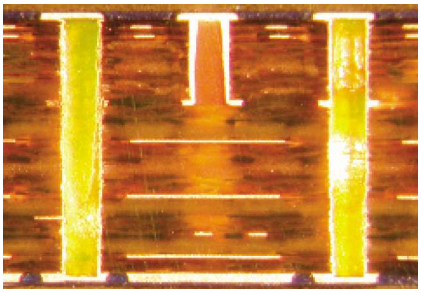
ring cost aspects this approach is scarcely justified anymore. New semiconductor technologies create (pose/present) design problems which so far didn't seem to exist. The consequences lead to complex multilayer systems securing functionality and EMC behaviour by a variety of measures.
The PCB construction is primarily based on three pillars: the hardware development consisting of schematic and PCB-design, the production of the PCB and last but not least the soldering and assembly of the devices.
It is obviously reasonable to keep the engineering of schematics and design as a company's core competence. However already in the design phase a close partnership with the PCB producer is indispensable. Additionally high pin count FPGAs in BGA cases and PCBs with 18 and more layers makes it necessary to choose the assembler carefully. These aspects have to be taken into consideration especially in research fields like the project UNIFIRE-II and the development of the CERO module.

Multilayer with appropriate EMC properties

Chip level aspects have to be dealt with by the semiconductor manufacturer. Nowadays substantially higher efforts in the development of PCB design and the construction of multilayer systems with appropriate EMC properties are necessary on the board levelThe compliance with the EMC guidelines is becoming increasingly problematic regarding the implementation of serial Gigabit transmission techniques.
High pin count FPGAs have to be handled, for example the Virtex II Pro from Xilinx offers up to 24 bi-directional transceivers each with 3 Gbit/s transmission rate. In this physical environment only sophisticated measures secure the smooth interaction of digital and analogue structures on one and the same PCB. Particular attention has to be paid to the number of layers for the power planes and their stack-up if different operating voltages are used. Core voltages down to 1.2 V and current transients of up to 50 A/ns are already common. Due to this development within the last few years the mere placement of single block capacitors or even groups of capacitors with the popular values of 100, 10 and 1 nF will not meet the requirements anymore. Currently consistent solutions are extremely seldom in high speed products.
Besides rising clock rates the short rise and fall times of the associated components lead to high speed designs meeting significant requirements. The demand for high signal integrity combined with low voltage power supply systems includes impedance controlled transmission lines with exactly matched delays. Especially the inductances of conductors regarding broadband decoupled power supply systems have to be observed.



■ The CPU module CERO: In this 18-layer board stacked power planes are realised as well as multistage decoupling of power supplies and impedance controlled conductor design



■ Decoupling of different power supplies of BGAs and GHz-frequencies are requesting new solution like plugging of PCBs

The cooperation with the CEM and the PCB manufacturer

The selection and placement of capacitor groups considering their conductor paths and the way to connect them to the powerplanes are essential. The blocking of different voltages of BGAs with 100 and more pins as well as clock rates in GHz ranges affords a completely new approach which can hardly be achieved with common CAD-strategies. Only the intense cooperation with the PCB manufacturer opens possibilities to work out processes like "PCB-plugging" or "stacked powerplanes" in an economically justifiable expenditure (see also part 2 of the series).
Equally important is the service provider for the assembly of the PCB. The completion of the design relies on supplementing information from the manufacturer. The reason (for this fact is that): series production of multilayer boards with 18 layers and more requires a close cooperation with an excellent production partner regarding component mechanics, temperature profiles and stencil accuracy. This process knowhow has undoubtedly to be integrated into the design.
For high speed applications it neither is economically reasonable nor technically feasible to to get oneself out of it in a trial and error approach with an average of 7-10 prototypes while taking into account the respective EMC tests.
The interfering influences of high speed semiconductors can only be encountered by well-founded comprehension of the physical fundamentals and their effects. *(cm)* ■

unit^el: Specialized in hardware design

Located in Graz/Austria the unit^el group has been active in hardware development for three decades. Main business fields of the high tech company are the development and construction of FPGA based embedded systems in combination with high performance CPUs (e.g. ARM, Motorola, Hitachi and Intel).
The spectrum includes services from project orientated consulting on customer specific applications up to the transition into series production. New PCB design technologies in combination with special layer stacking for power supply planes result in impedance controlled PCBs with extremely high signal integrity up to the Giga-bit ranges and excellent EMC behaviour.

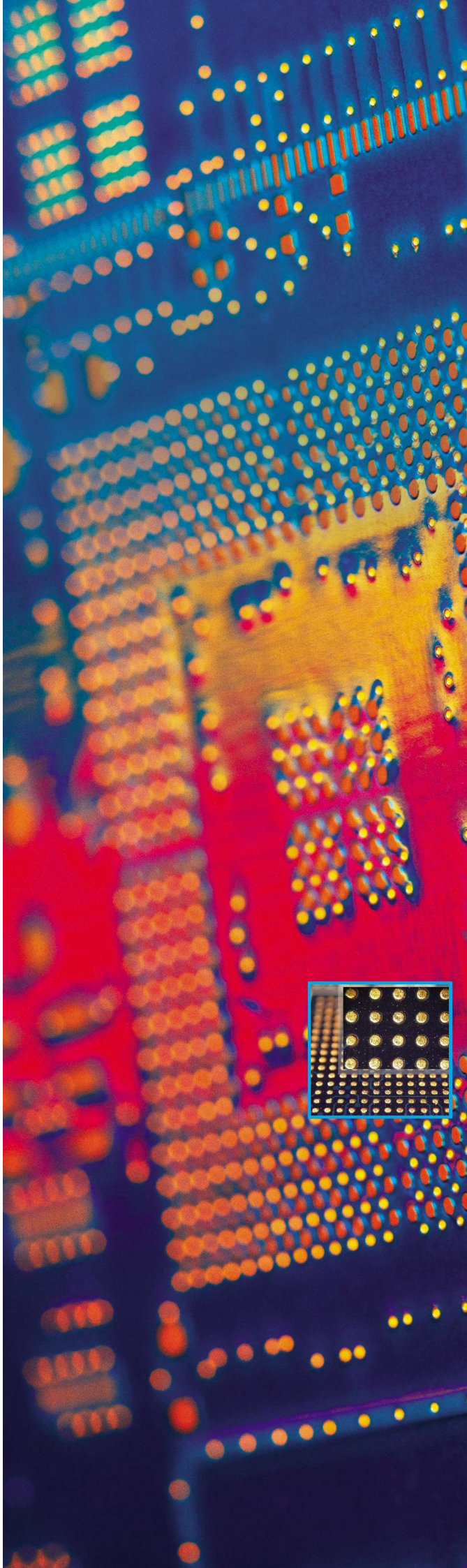
PCB design

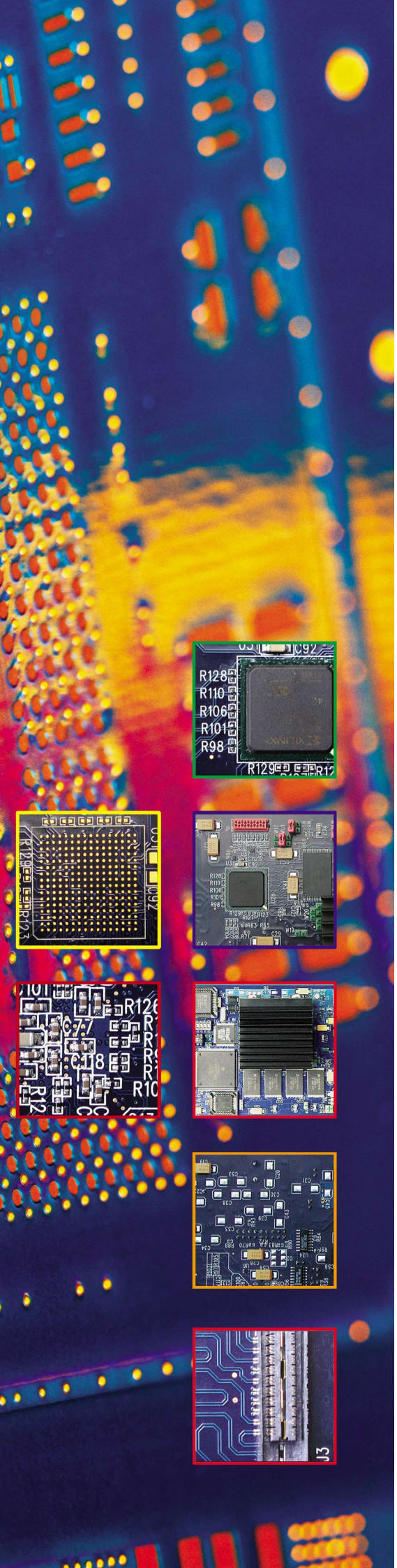
Breaking new Ground on Board Level

Besides being the circuit carrier and the connecting element the PCB nowadays has to establish stable conditions. The interfering influences of high speed semiconductors can only be dealt with a well founded comprehension of physical laws and their effects and conventional CAD strategies are no longer applicable. An example: Due to the reduction of structure sizes in VLSIs demanding a reduction of core voltages to 1.2 V and below, transient currents of up to 50 A/ns become the norm. Decoupling capacitors or groups of capacitors fail to meet the requirements. Additionally the cooperation with the PCB manufacturer becomes essential in order to stay within an economically justifiable time frame and to work out a feasible solution.

by Gerhard Eigelsreiter und Arnold Wiemers

In part two of our series we will look at the essential milestones within the development process by taking a closer look at the processor module CERO. The range of the functions of the processor module is determined considerably by a maximum life cycle combined with the topicality of development.
The term long life cycle is defined by including present as well as prospective interfaces that have not yet been invented and documented. Topicality is determined by the degree of integration into existing structures.
This procedure leads to a high degree of flexibility, but has an impact on the simplicity in the development. Well, how does the realisation look now?
The choice of the interfaces is crucial for a long life cycle as is the availability of the components. Standard interfaces enable immediate connection to a variety of devices.
A good mixture facilitates the incorporation into an existing hardware environment. Purely by the key element of bandwidth resources it is possible to quasi-integrate – through a kind of adapter – completely new or still not yet fully defined interfaces. By means of differential signalling with 32 point-to-point channels CERO achieves a maximum transmission rate of 25.6 Gbit/s. That's enough to include for instance 10 Gbit Ethernet or fast Fibre-Channel and Firewire connections. Interfaces to PCI-Express and Hypertransport on the PC-side can be realised as inexpensively as RapidIO on the embedded





side. Therefore high performance and flexible ICs are needed. The individual project steps keep to a norm: Breaking the functions into individual hardware components and their connections down on the printed circuit board. According to a standard scheme the functions are fractured into individual hardware segments and their connections on the PCB.
Starting with the choice of the components and the creation of the schematics the procedure continues with the transfer into the PCB design, the production of prototypes, initial operation and functional tests – and finally the inevitable small amendments in design and schematics. Ready!?
And where does physics come in?
If at all it is considered rudimentary in the design stage or at the obligatory EMC test – anyway definitely too late. It is still possible to get somehow along with the EMC tests with sophisticated shielded housings, ferrites and suppression chokes – however at the expense of stable functionality.

The new role of the PCB – providing stabile regions

Multiple interfering elements can be foundon the PCB. Shielding measures such as special housing materials that are placed later may reduce emissions outside the housing but not on the PCB itself.
We have come to the conclusion that the origin of radiation has to be avoided. This is hardly possible except by switching off the device or the radiation has to be absorbed at the sources.
Thus the PCB besides being the circuit carrier and the connecting element plays a third, elementary role: providing stabile regions with controlled calm conditions. This is particularly relevant for critical circuit parts, especially when VLSI-semiconductors are used. Such sources of interfering radiations should be defused as close to the source as possible. The chip itself would be ideal but more or less conclusive reservations on the part of the manufacturers are the obstacle.
CMOS-VLSI Circuits are generating peak currents of 50 A/ns and more. Suitable measures are implemented directly at the supply pins to diminish the spread out (the spreading out) of reflections on the power planes. Additionally the number of necessary voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V) is increasing steadily due to ever smaller semiconductor structures. The avoidance principle applies.

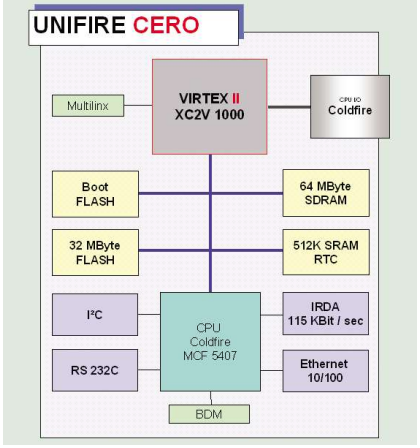


Figure 1:
The processor module CERO: Scope of functions of the processor module is determined by an as long as possible life cycle and actuality of the development.

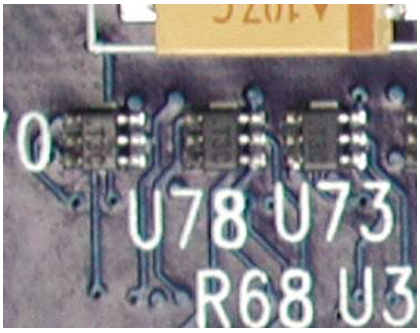


Figure 2:
Active termination chips on bus connections are improving signal integrity significantly

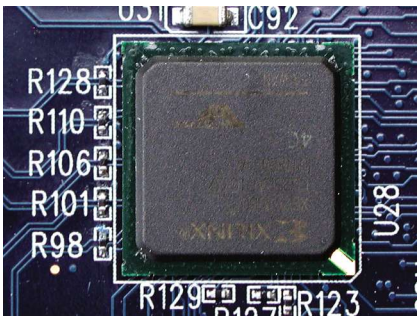


Figure 3:
The Virtex-II FPGA comes up in a BGA case

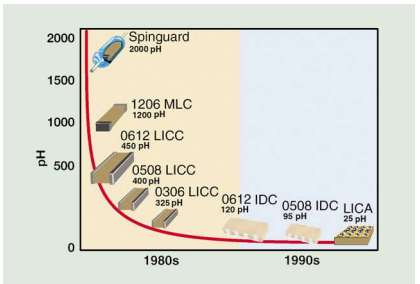


Figure 4:
LICs (Low Inductance Capacitors) from AVX

Careful component selection

A careful selection of all components forms the basis. The focus lies on a fair balance of arithmetic performance and memory capacity in relation to the transmission capacity and speed of the interfaces. As transmission rates in Gbit/s ranges cause a drastic reduction in the choice of suitable ICs, programmable logic (PLDs) become obligatory.
The performance of the CPU isn't the main criterion anymore. The arithmetic hardware performance of complex PLDs allows the implementation of embedded controllers even in mid-range applications from 200 MIPS onwards. The main advantage lies in the use of long-term approved software development tools (C-compiler, operating systems etc.).

Choice of the PLD is determined be the desired function

The selection of the PLDs is determined by the desired functions. Partially reconfigurable and reprogrammable FPGAs have been chosen.The necessary amount of LVDS based interfaces (module ITRIX) determined the implementation of Xilinx SRAM based FPGAs (e.g. Virtex-II Pro).
A further decision criterion was the experience of many years in handling the development tools. A broad range of embedded controllers is supporting the performance in the 200 MIPS range. Our knowledge based on two decades' experience in the handling of Motorola CPUs has led to the implementation of the MCF5407-Coldfire component.
The "Glue Logic" interconnection logic requires special attention. The avoidance principle requires substantial concessions. Interfering radiation can be controlled best if it doesn't occur at all. However the necessary interconnection by means of busdrivers and logic gates (CMOS) can increase to 1st grade noise sources. It wouldn't have been the first time that fast CMOS logic causes EMI measuring results that give you a nightmare.
Therefore we opted for analog multiplexers and switches. FPGAs, CPUs, Flash RAMs and SDRAMs are hardly to be avoided. For this reason modifications are necessary. Tremendous opportunities in schematic draft make FPGAs the first choice, particularly for using the avoidance principle purposefully, after completion of the PCB e.g. by means of differential transmission techniques. In contrast microcontrollers cause significantly more problems. Particularly persistent cases probably require the change of the ▶

The PCB for UNIFIRE II/CERO

Arnold Wiemers, ILFA GmbH, has optimised the production parameters for the CERO processor PCB.
Even in these days a PCB with 18 layers is quite a challenge. For the project UNIFIRE II additional tasks are a multi-power-system, differential impedances, blind and plugged vias. Power supplies around 3.3 V with highest requirements in reliability during operation as well as extremely reduced electromagnetic immissions and emissions can only be achieved by UTMs (Ultra Thin Multilayer-boards).
The nowadays producible minimum spacing of 50 microns between adjacent power planes combined with a sophisticated VCC/GND distribution promises the realisation of the requested stabile power supply. Some of the planes additionally serve as a reference for differential signals. The power supply pins of the components placed mainly on the TOP layer had to be connected to the various power plane layers by vias. Further requirements led to sequential vias from layer 1 (TOP) to layer 9 and certainly there were still the obligatory vias from layer 1 to layer 18 (BOTTOM).
Therefore a conventional layer stack-up with inner cores was not possible. Pre-production discussions determined a multilayer construction of 2 3 9 layers, meaning to produce two

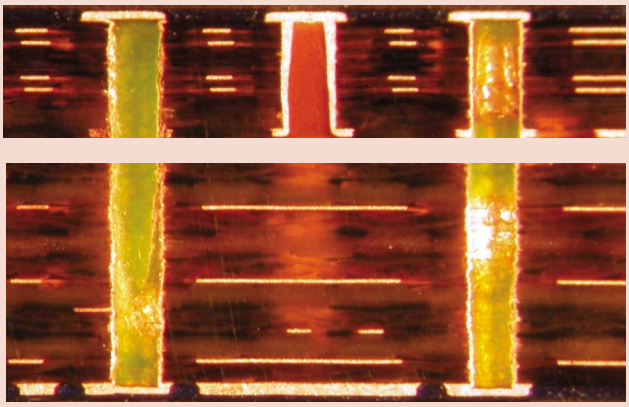


Figure 1: UNIFIRE II/CERO consists of 2 × 9 layers being pressed to an 18 layer board

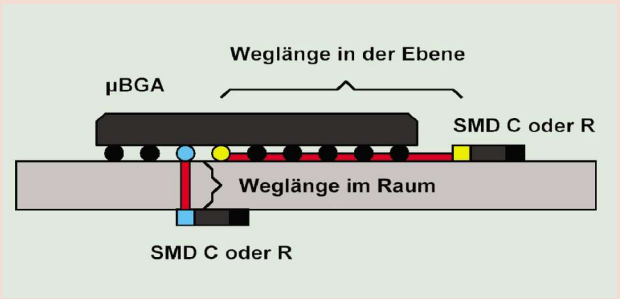


Figure 2: Using conventional connecting methods lead to relatively long traces between ICs and passives compared to a 3-dimensional wiring

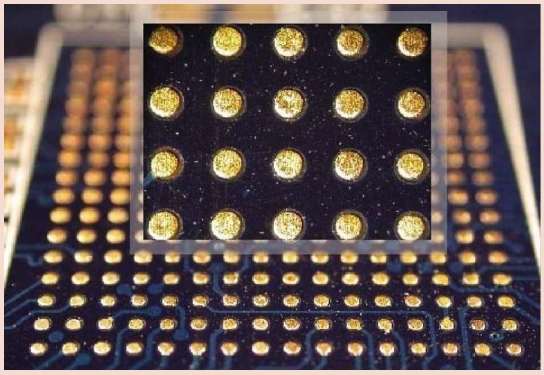


Figure 3: Drills in the BGA-pads are through holes and by means of plugging filled from TOP and BOTTOM

separate multilayers to be pressed together to the final 18-layer board in a second production step.
Thus the problem with the sequential vias from layer 1 to layer 9 was solved because these quasi-blind-vias could be handled as through holes in the first partial multilayer. These vias (if they were to be produced as "real blind vias") could not be elaborated by laser due too poor quality of the barrel and the too high drilling depth. Alternative mechanical drilling is not advisable regarding the aspect-ratio. Severe problems during the plating process are to be expected.
The second partial multilayer from layer 10 to layer 18 was conventionally produced and didn't bear any peculiarities. These layers mainly served as signal layers and therefore allowed the construction consisting of standard materials, last not least because a final board thickness of 2.2 mm should to be achieved.
Regarding PCB technology this stack-up causes complications resulting from asymmetry and the two pressing cycles. Possible twist-and-bow effects due to the asymmetrical stack-up can be reduced widely by intense tempering of the used cores and prepregs as well as by applying a raster to unused areas on the inner layers outside the actual PCB to achieve a greatest possible identity in copper and non-copper shares on each layer to minimise tensions during the pressing cycle. The expected warp due to two pressing cycles as well as for the same reason reduced layer distances can only be estimated on the base of experience.
An exact calculation is not possible because of individual layer distribution, distances and pattern structure. Experiences made during the first production run have to be implemented into the defaults for compensation factors for the cores and/or for the d-code correction for the trace width of the impedance controlled connections. After having pressed the two partial multilayers together the PCB production is proceeded "as usual".
UNIFIRE II is a high speed application. Significant requirements are therefore impedance controlled traces, observance of signal delays, the necessity of high signal integrity in spite of low power supply voltages and attention upon the inductance of the connections.
Due to the component geometry conventional routing leads to relatively long traces between BGA or chip and the passives. To allow a 3-dimensional placement and routing the UNIFIRE II PCB was completely plugged. At first sight the placement resembles being a conventional double-sided SMD assembly, but actually it is significantly different.
TOP-BOTTOM-connections are not realised in the classical stair-like via-track-via version, which probably leads to discontinuities, but the via itself is the connecting trace. The maximum connection length corresponds to the final thickness of the multilayerboard, in this case 2.2 mm.
The BGA-connections to the periphery therefore are extremely short, parallel, equal in length, not crossing each other and do not follow the traces of other signal pins. In case of CERO via holes in the BGA pads were through holes and closed from TOP and BOTTOM by plugging. Thus the BGA solder land faces no hole at all but a flat and continuous surface (see fig. 3). The tool defaults for films and templates, necessary for the plugging process, were elaborated out of the provided CAD data at our CAM system. Additional plating in context with the plugging process however causes restrictions. Regarding the etching of the pattern on the outer layer the normal copper thickness of at least 42 micron (resulting from 17 micron base copper +25 micron plating copper) actually is already too much. Due to additional plating during the plugging process this copper thickness is increased by another 15 micron. Etching resist and etching process therefore become important.
Beyond that also the influence of the abrasion procedure is to be considered, which is necessary for removing the arrears of the plugging substrates. Abrading causes a not precisely predictable and unequal final copper thickness with possible deviations from 5 to 20 micron. The different copper thickness impairs the etching results which can only be controlled optimally in case of an equal copper thickness. Copper layer abrasion has influences even on the conductors cross section on the PCB.
Current carrying capabilities, trace resistances and impedance controlled signals are subject to a wider tolerance field. Especially differential impedance is sensible to unintended variation in pre-calculated copper thickness, etching tolerance range, trace distance and mechanical distance between signal layer and power plane. Measuring test coupons out of the production panel before and during the etching and abrasion processes supplied accompanying and helpful information concerning mechanical proceedings. On the background of proved experiences from other projects the required differential impedance of 100 Ω (±10% usual tolerance) could be achieved at the first attempt.

PCBs on high technical level

"We always aim to be in a leading position in advanced technologies", is ILFA's philosophy. ILFA Feinstleitertechnik in Hannover, Germany is recognized as a manufacturer of PCBs on a high technical level and plays a leading role in HDI-(High Density Interconnect) PCBs and flex/rigid-flex application.
Founded in 1979 the company's staff consists of 130 employees. ILFA GmbH is seen as a specialist in prototyping as well as series production and special solutions. Besides PCB production business fields are CAD design, solder paste stencil manufacturing and CAM tooling.

According to our opinion UNIFIRE-II/ CERO is quite a pretentious multilayer. The fact that this PCB could be manufactured successfully and practically without any complications from the start is worth to be mentioned and is to be attributed above all to the co-operation between the partners involved. We are convinced by the commitment of unit^el and wish them all success.

The PCB 2005 circuit design system represents an integrated way of viewing electronics design that has been implemented through a partnership. It covers component selection via a design that is compliant with EMC regulations and ensures the functionality of the unit right up to the manufacturability of the PCB. Last, but not least, it covers the mounting of the components onto the assembly unit.
However, a good EMC performance is also required to guarantee stable operation of the equipment. Hence the PCB no longer acts merely as a mechanical carrier for the components and the electrical interconnections, as the design also covers the need for stability in the presence of interference and reduces electromagnetic immissions and emissions. Anyone who believes that such systems are still far in the future is mistaken.
With clock rates starting at 400 MHz and with signal rising and falling edges of 3 ns duration, high speed circuit design is essential. There are several ICs already on the market that operate with signal slopes far shorter than 1 ns. In order to meet these requirements, approaches must be made at board level, as conventional CAD strategies are incapable of achieving them.

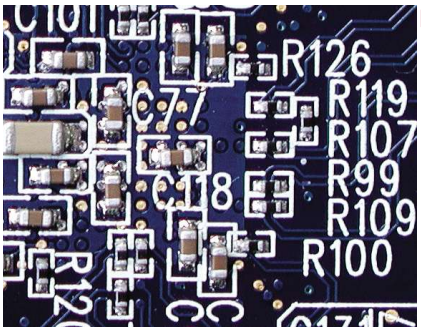


Figure 5:
SMT-decoupling-capacitors are placed on the backside of the PCB directly under the FPGA

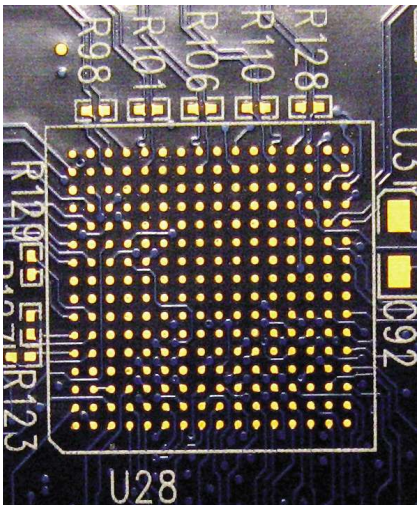


Figure 6:
Component side for the Virtex-II BGA with 256 pins

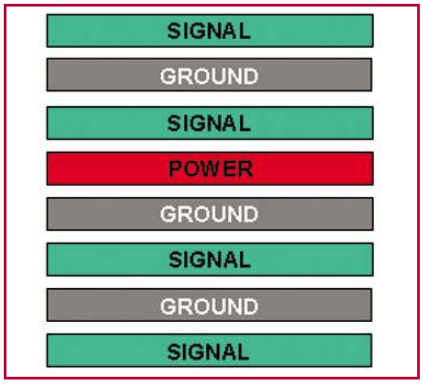


Figure 7:
General PCB Stack-up for impedance controlled PCBs

component manufacturer. Regarding this Flash RAMs and SDRAMs are less critical in handling. Unfortunately, relevant references are nearly completely missing in the data sheets. Constructing prototypes and the following measurements seem to be the only solution. Impedance discontinuities of such bus related systems can be tolerated easier by an active termination.

New PCB-technology and connecting techniques

Now, how can a solution be reached, if hardly anything can be avoided – if, so to say, the "Formula-I-racing car" in hardware with transmission rates of several Gbit/s is to be realised? And at the same time a change to a different type of CPU with relaxed EMC-behaviour for specific reasons is not possible?
A readymade solution cannot be offered, but a promising approach: broadband power supply decoupling on the PCB, accompanied by measures on design level and a special stack-up (piled power-planes).
A proper extent of risk taking and a PCB manufacturer who loves experimenting are the ingredients for research in a field which is not the core task of electronic development. Research in new PCB-technologies, layer Stack-ups and connecting techniques have led to a high extent of information exchange over months.

Broadband decoupling of power supplies

Complex, high pincount FPGAs are preferably delivered in BGA cases. Low voltage power supplies combined with increasing supply-current requirements represent new challenges.
Additionally FPGAs, depending on the circuit design, are known for significant rapid current changes in the range of several amps. Due to insufficient decoupling and triggered by low core voltages (1.2 V) with tight tolerances the infamous voltage drops occur, having great impact on functionality. Additionally all of the existing power supplies are affected considerably.
Classical decoupling methods consist of electrolyte and tantalum capacitors for lower frequencies and ceramic SMT capacitors for frequencies of up to 10 MHz. As a third element the PCB, providing power supply systems as planes for frequencies from 10 MHz up to several GHz, becomes increasingly essential. These figures for the frequency don't describe the clock rates as often is mistakenly believed but the critical frequency during the rise and fall times of the signals.

The capacitor is an ideal decoupling element

Even in a moderate 10 MHz system frequencies of 100 MHz and more that cannot be neglected are found. The capacitor is an ideal decoupling element. Unfortunately it is impossible to buy such a capacitor. Only a mixture of inductance, resistance and capacityis available. In the manufacturers' data sheets the term ESL (equivalent series inductance) describes the share of inductance – the smaller, the better. By intensively searching the net

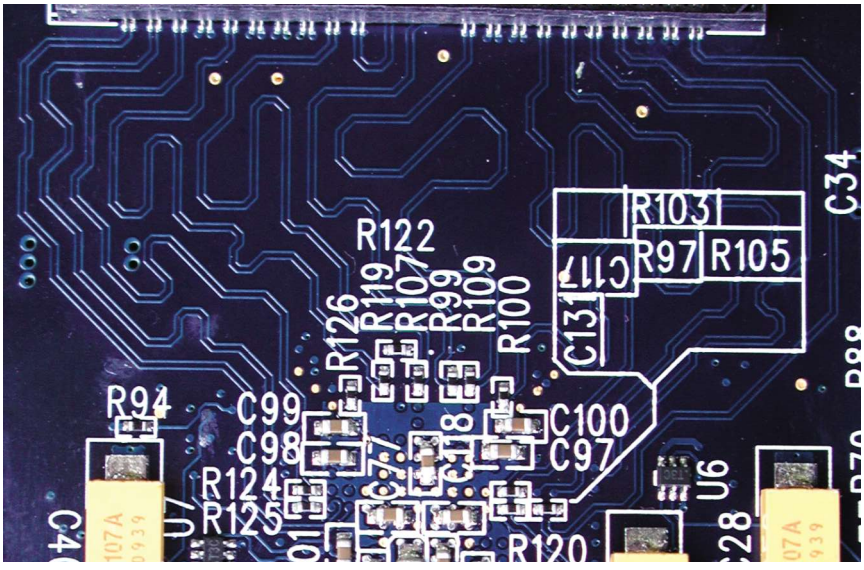


Figure 8:
Routing of 40 LVDS connection pair offered unknown possibilities to explore personal limitations

you can find capacitors with ESL values of less than 400 pH – customized below 30 pH.
According to the manufacturers' application notes they are to be placed as close as possible to the power pins. But what does "as close as possible" mean in practice In fact all semiconductor manufactures remain more or less silent concerning the practical realisation, however design recommendations are occasionally made but altogether they do not disclose too much. A ceramic capacitor of 100 nF has en ESL value of about 1200 pH. A via hole of 1.6 mm length adds about 1000 pH.

Capacitors directly placed on the vias of the BGA Vcc pins

The solder balls of a BGA case make you think of a fakir's bed. Despite the fact that there are placing possibilities at the edge of the BGA cases most of the power supply pins are located in the middle. It doesn't make sense to apply capacitors with ESL values of 400 pH and less when the connecting conductor lengths and vias add up to inductances of 10 nH and more.
Considerable improvements can be achieved by placing the SMT capacitors on the back of the PCB directly on the vias of the BGAs Vcc pins (1.5 V). However, this "plugged via technique" depends on the manufacturers' open – mindedness to new ideas and his good will to develop and apply new methods. Distinct requirements are set for the board assembler as well (see part 3 of the series – page 72).
Correctly constructed power planes produce a high-quality area capacitor for high frequency decoupling. But caution: They are not a universal remedy even if construction and Stack-up are appropriate. Physics show particular moody behaviours: capacitor groups becoming inductive can develop risky parallel resonances causing considerable problems even in case of appropriate layer stack-up of Vcc and GND planes.

Build a correctly dimensioned power supply system

I.e.: To build a correctly dimensioned power supply system these groups have to be calculated. Undesired impedance increase at certain frequencies can be reduced by thin cores in Vcc/GND plane systems combined with adjusted capacitor groups. Further optimising possibilities are provided by piled power planes. Those are constructions which behave like Vcc/GND plane system consisting of extremely thin cores that cannot yet be produced.
Arrangement and stack-up within he PCB, which have to build an entity, are crucial. Anyhow, these advantages have to be made up for with a higher number of layers (in our case 18). However, additional costs amount to merely a fraction of the costs which are necessary to remove instabilities, not to be mentioned the loss of time if products miss their launching date.
Several ornamentations here some free areas there – the autorouter again has produced a fancy result. Almost everyone has experienced such a scenario. These negligences can't be compensated with any decoupling concept, no matter how superb it might be in other circumstances, because even the Vcc/GND planes of power supply systems behave like conductors with open ends.
A whole bundle of connections has to be placed on the board with a variety of rules and restrictions to secure signal integrity.
There is no way – thoughtless procedure is not supported!
The routing of 40 conductor pairs (including controls) to realise LVDS transmission techniques in a point-to-point connection with channel capacities of 800 Mbit/s (here we were supported by our cooperation partner WEDAsoft located in Baden/Austria) was really thrilling. Impedance controlled PCBs were inevitable.
A lot of arithmetic exercise and constant coordination with the PCB manufacturer has led to optimal and above all viable results.

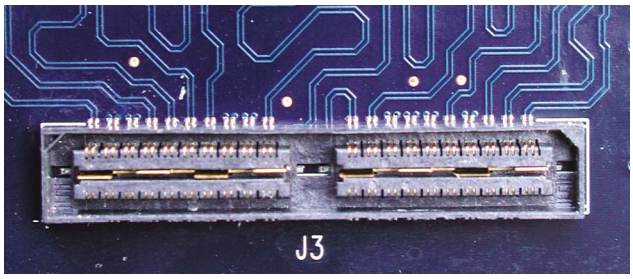


Figure 9:
PCB connector for 40 LVDS connection pairs

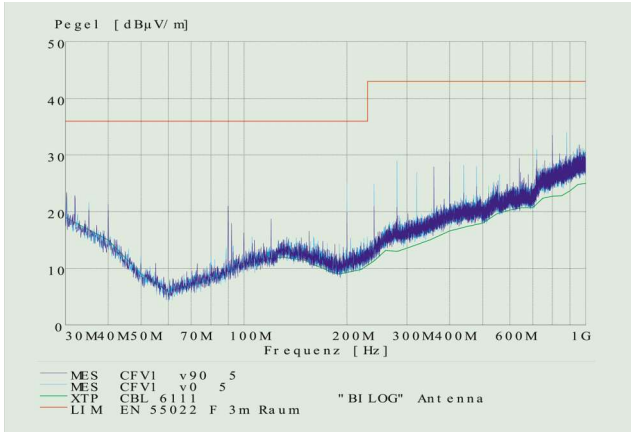


Figure 10:
First EMI-measurements with-out housing and external shielding. External CPU-Clock 40 MHz, internal CPU-Clock 160 MHz, internal FPGA-Clock 200 MHz (DCM-multiplier 5)

Minimise skew for synchronous data transmission

Close tolerances and trace length differences of less than 0.5 mm between the conductor pairs as well as length differences of less than 0.8 mm among each pair guaranteed minimised skews for synchronous data transmission. Different delays of signals on inner and outer layers has led to a fast increase of optimisation runs and changed the designer's gloomy mood.
Impedance gaps were reduced by selecting suitable connectors and forbidden layer changes between the two endpoints of the conductor pair were avoided.
The results, supported by measurements wholly justify the efforts taken.
Many control sessions later it was time for the PCB manufacturer ilfa to recover – but now it was the contract electronic manu-facturer's TAUBE ELECTRONIC turn to start working. *(cm)* ■

PCB assembly & starting up

The Moment of Truth

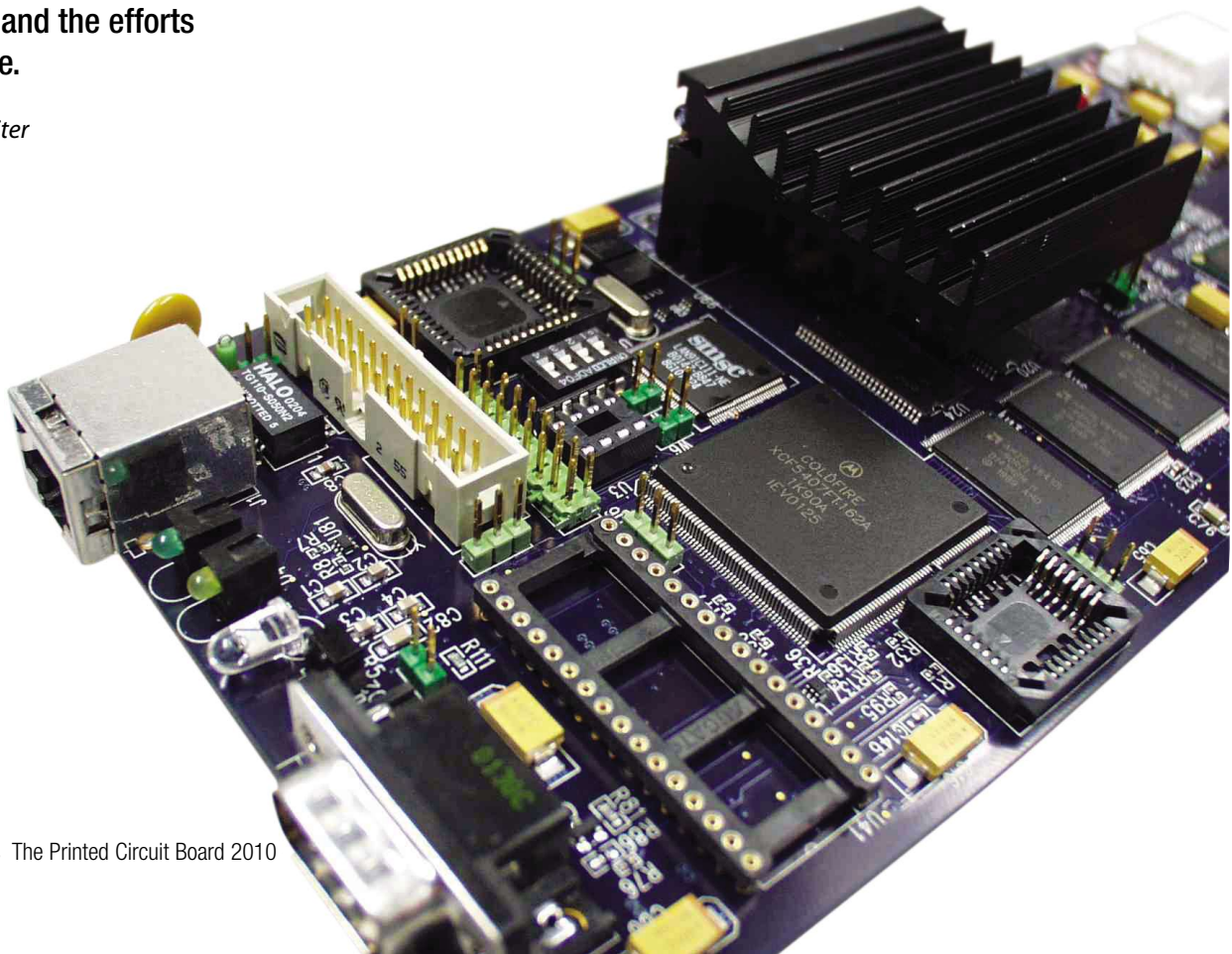
An interface-independent core hardware which combines a powerful CPU with dynamically reconfigurable FPGAs and thereby provides high I/O-bandwidth which can be used in an unrestricted way – this idea was to be realised by the CPU-module CERO. The combination of flexible soft- and hardware, I/O-bandwidth, extensive constructive measures in the field of PCB-design, optimising strategies of the PCB manufacturer and the board assembler in an interplay of schematic draft and PCB-design elaboration set new benchmarks regarding stability and functionality of the hardware – and the efforts were worthwhile.

by Gerhard Eigelsreiter and Thomas Thun

After the completion of the PCB for the CERO-module – an 18-layer-board with piled powerplanes, differential impedances, blind vias and plugged vias – it has to be assembled. Normally the board assembler faces the accomplished facts and is confronted with the completed PCB. Well, it's not surprising that some of the electronics manufacturers finally behave as moody as physics in GHz-ranges. In order to prevent this the cooperation of unit^el, ILFA GmbH and TAUBE ELECTRONIC was planned right from the start and the exchange of information has been successfully inplemented .
The employment of new technologies in PCB construction, the insertion of components with very small packages and high pin counts has to comply with the production possibilities of the service provider. Especially regarding ICs in high-pin-count BGA packages the plugged-via-technology demands a precise coordination between board assembler and developer concerning land pattern dimensioning and the SMT capacitors. This information is already implemented into the PCB design when creating the component library of the PCB design tool. Finally after a modification of the land pattern of the SMT capacitors the board assembler agreed to the plugged-via-technology. The precision of solder masks, the component distances and density are no more than an extract of a set of rules that significantly contributed to the solder- and production quality of the assembly.

Realize a PCB-design for manufacturing

An 18-layer-board with piled powerplanes puts the cooperation between PCB manufacturer and electronics manufacturer on a new, and in terms of quality higher level. At this stage measures against twist and bow during the solder process are determined as well as solder samples have to be provided to investigate optimised temperature profiles.



Setting-up operation

Finally dinner is served – the most interesting part for any hardware developer is setting-up operation, even the slightest mistake is relentlessly detected. Due to the complex PCB layer stack-up the electronics assembler suggested producing only one prototype instead of three giving the possibility to fall back on two complete component sets for a fast implementation of possible changes.

A resulting disadvantage: During setup no comparing measurements were available, giving the situation – to put it mildly – a decent exclusiveness with temporarily shifted culmination points. The 3.3 V operation voltage was externally supplied through a 3-pole power supply connector. On the board itself two linear amplifiers generated the additionally necessary 1.8 V core voltage for the Coldfire-CPU as well as the 1.5 V core voltage for the Virtex-II FPGA.

This sequential enabling of the voltages solves a critical problem required for the Coldfire "power-sequencing". The 1.8 V have to be available before the 3.3 V. An auxiliary logic ensures the adherence to the maximum voltage difference of 1.8 V between core and operating voltage even during switching off . The core voltage of the FPGAs was not subject to these restrictions. A first attempt success (a first go success): the first prototype works

Using a regulated power supply unit for general laboratory applications with adjustable current limit the operating voltage was slowly raised towards the targeted 1.5 V. Initiated by a sharp current rise beyond the expected limit already at a very low initial voltage, a short troubleshooting session revealed the following: Instead of the expected 1.5 V at the first testinstance the current rose very rapidly to 1.5 A (expected value 0.6 to 0.8 A). Despite careful insulation a body contact heat sink – linear regulator could be detected, which could be eliminated immediately. Then all measured values lay(were) in the expected range – the operational current amounted to 0.6 A.

Apart from a redundant additional SELECT line to the SDRAM controller of the Coldfire-CPU and the logic level change of a control line in the newest data sheet revision of the Ethernet controllers the remaining tasks, from the hardware point of view could easily be executed right from the start.

And all that – it has to be pointed out – by means of this one and only prototype. There is nothing worse than adapting new firmware on to hardware, which exhibits soldering and assembly errors.

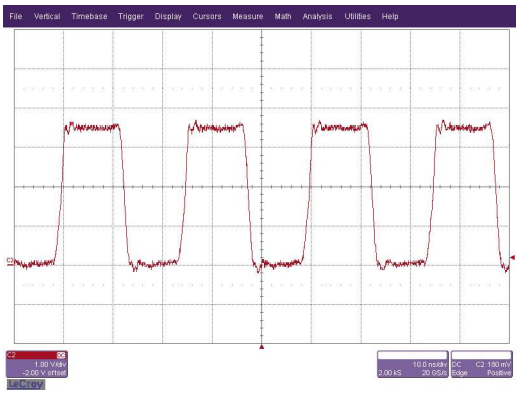


Figure 1: System clock 40 MHz measured before the clock-distribution; all clock-lines are active terminated point-to-point connections

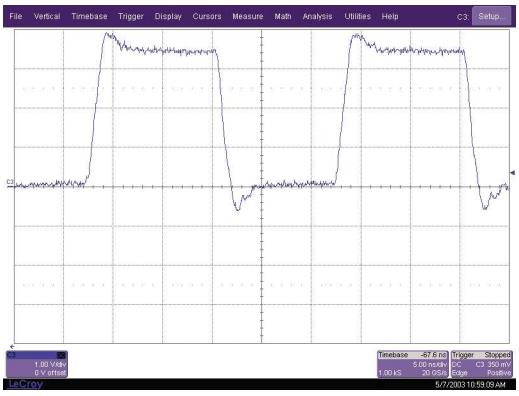


Figure 2: CPU-Clock 40 MHz behind clock-distribution at the end of the connection; the effects of the active termination started on an average of 0.6 V of the respective logic level

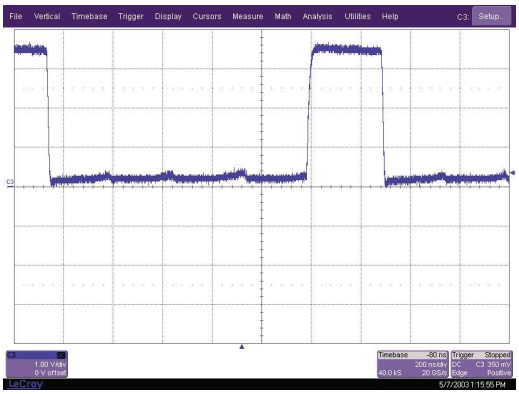


Figure 3: Measurement of data signal D28 at the system-data-bus; all bus systems as well as all SDRAM controls are active terminated

Combination of CPU and FPGA pushes debugging of hardware and software

Meanwhile the software department had to face completely different problems. Incomplete or contradicting RESET and initialization sequences in the manuals and application notes delayed the compilation of the firmware. The BDM-Interface to the Coldfire-CPU turned out to be a great help. In principle it represents a simple analyser built into the CPU chip.

It offered extended possibilities of loading programs, examining program sequences, on-the-fly debugging, examining and of changing register values as well as visualising important internal structures.

Significant enhancement in hardware and software debugging pushes the combination of CPU and FPGA by means of arbitrarily reloadable, free contrivable analyser modules.

Even high-complex, sometimes extremely fast timing sequences can be represented by testpoints and connectors (easy accessible for probes) without having any influence on critical signal delays or changing real time operation behaviour. The simulation of the adjustment of different setup and hold times in the timing of the Ethernet-controller and the Coldfire-CPU could therefore be examined by measuring on the target hardware in real time without disturbing factors that are otherwise inevitable

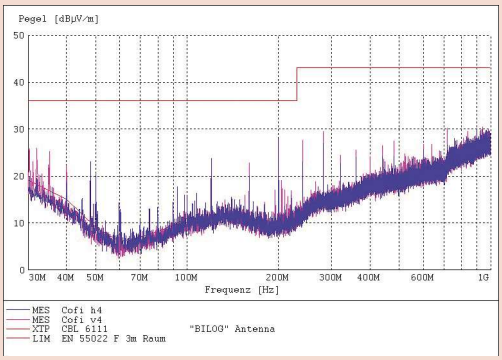
Signal-integrity measurements

A further delicate topic in hardware design are the measurements concerning signal integrity. Signal paths, which are subject to signals with high slew rates, have to be designed as wave guides, i.e. with controlled impedance. This seems to be a textbook note – and it actually is – Considering point-to-point connections these requirements can be approximated in their simplest form by impedance controlled wiring and a serial source resistance. What does the textbook say about bus-driven connections?

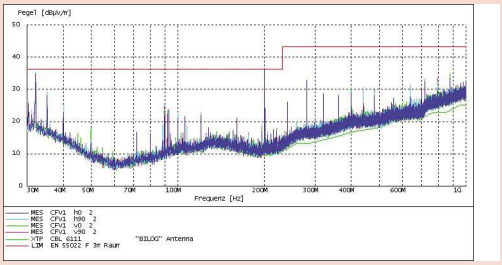
Interference measurements of UNIFIRE II/CERO in frequency ranges between 30 and 1000 MHz

Thomas Thun, associate director of the State Institute of Electrical and Electronic Engineering and Accredited Test Laboratory TGM in Vienna, had measured the interference radiation of the CERO CPU module.

The major challenge for hardware developers to comply with the EMC guidelines in case of printed circuit boards with I/O bandwidths of several GHz definitely is the adherence of the radio interference field-intensity limit values in the frequency range of 30 to 1000 MHz. From the beginning attention has to be focused on the EMC problem to avoid being confronted with insuperable intricatenesses in posterior development states.
In case of the measured 18-layer board UNIFIRE II/CERO latest cognitions in interference reduction and noise rejection were introduced. These measures have nothing to deal with conventional RFI suppression (insertion of capacitors, chokes and ferrites). They mainly take place inside the PCB design structure and therefore are irrevocable.
For the purpose to evaluate the radio interference field-intensity of UNIFIRE II/CERO the European Standard EN 55022 "class B" (applies to domestic environment) was consulted. The measurement was executed in the shielded absorber chamber at the TGM in Vienna. In order to sum up the so-called worst-case-scenario (the radiation of electromagnetic energy does not occur in equal intensity in every direction) the PCB was mounted on a rotary platform at a distance of 3 m to the measuring antenna in order to be gauged in all directions.
To record the polarity of the emitted electromagnetic radiation the measuring antenna itself (a combination of a logarithmic-periodic and a biconical antenna) had to be turned into the vertical and horizontal plane. The graphs in the measuring diagrams figure out the respective radio interference field-intensity in the frequency range of 30 to 1000 MHz for the different positions of the Reprinted Circuit Board and the correspondent polarity of the antenna. Additionally in the measurement diagrams the threshold value in consideration of the correction factor for the Ground-plane measuring method is shown as a line (see figure 4 and 5).
It is obvious, that the results clearly fall below the threshold values, as well in horizontal as in vertical polarisation over the whole frequency range. This instance gains importance, because the PCB measurements were performed without any shieldings or housings. CERO complies with the requirements of European Standard EN 55022 and therefore the EMC guidelines.



■ Figure 4: Interference spectrum of the CERO module without housing and without external shielding measures: The test-software was a specially for the MCF5407-CPU programmed SDRAM memory test at a system clock of 40 MHz and an internal CPU clock of 160 MHz



■ Figure 5: The acid test: more than 9000 CLB-flip-flops were synchronously switched at rising edge with 200 MHz global internal system clock. The measured current rose from 0.9 to 4.6 A. The 200 MHz line nearly reached the limits.

▶

Wellthis is difficult to say! Actually this answer isn't really helpful to solve the problem. The use of active termination chips, at the end of each bus connection as well as in the middle represents a good compromise.

Caution when using active termination chips

However optimum performance of these termination chips can only be gained in case of excellently decoupled power supplies. On the CERO module all clocks are point-to-point connections with active termination at their respective end. The system clock is lead (is guided ?)via a clock distributor, its outputs being connected by delayequalised traces to the CPU, the FPGA and the SDRAMs. All SRAM controls are terminated and certainly all bus connections are actively terminated as well.
The 6-GHz-high-speed-oscilloscope WaveMaster 8600A from LeCroy, being predestined for jitter and timing analysis, was used for clock and data signal recording and evaluation. The impedance of the signal traces in relation to the power planes plays a decisive role concerning the function of the device.

Each differential conductor is referenced to groundplanes

Therefore each differential conductor pair is referenced to one or two groundplanes. Differential impedance averages out at 100 Ω. Using the impedance calculation software from Polar Instruments Ltd., mechanical parameters of the conductors, such as width and copper thickness associated to the layer distances, were determined by the PCB manufacturer and transferred as constraints into the PowerPCB layout tool. Equally all single-ended signals are referenced to the respective Groundplanes, thus optimising the current return path – verified by the appropriate measurement results.

■ EMI measurements

Measurement results concerning waveforms of critical controls, e.g. clock lines of CPU, FPGA and SDRAM, not only suggested excellent signal integrity, but also have given room for cautious optimism regarding the coming EMI measurements. Cautious optimism, because particularly switching characteristics slope and dynamic power consumption of highly integrated CPUs and FPGAs affect considerably the degree of radio interference. However, the excellent stability

and functionality of the hardware turned out to be the much more important detail. Intricate testing up to the load limit carried out over months has not led to instabilities or data overruns in a single case.
The FPGA test scenario represented a special challenge. By software shifting more than 90% of the available CLB-flipflops (approx. 9000), were clocked by means of DLL over the global Clock network with minimum skew in parallel with 200 MHz. The measured operating current abruptly rose from 0,9 to 4,6 A. An appropriate heat sink for this „High-Frequency-Heater" (FPGA) kept the temperature within the limits given by the manufacturer.
Irrespective of that the acid test for the SDRAM was run on the entire 64-MB-memory via the CPU. All test scenarios were connectible and disconnectible (could be connected and disconnected) arbitrarily by software. (Figures 4 and 5, contribution page 72).

Combination of a high performance CPU and dynamically reconfigurable FPGAs

Where will all those efforts lead to? With all that technical enthusiasmone should not forget the underlying purpose of the efforts: the application itself. The combination of a high performance CPU and dynamically reconfigurable FPGAs paired with an extremeley high I/O bandwidth that can be used for the application without any restriction to realise a hardware whose application fields cover many market segments. There is no focus on a certain operational area . This is exemplified in the article on image processing on page 59.

Epilogue

Finally only practical experience and the market can serve as indicator for the suitability of consistent approaches. The magic word bandwidth with an emphasis on the I/O-area increasingly proves as the linchpin for flexible core hardware with long life cycle in market segments with rapidly changing product cycles and adaptations. The following example will give you proof of this. In May 2003 Xilinx presented their own transceiver-IC's (RocketPHY) with 10 GBit/s for serial data transmission (White Paper: Backplane).

20 LVDS input and 20 LVDS output channels at free disposal

The parallel connection to 16 LVDS input and 16 LVDS output channels of the Virtex II (PRO) product lines specific to the chip. By a specific connector, optimised for differential signal line guidance, the CERO board provides even 20 LVDS input and 20 LVDS output channels (including controls) at free disposal. Necessary layer changes of LVDS pairs to the inner layers were realised exclusively with blind vias, "back drilling" was out of question [1].
Although the development of this board is based on design documents issued at the beginning of 2002, the degree of freedom concerning hardware changes with a view to further bandwidth requirements have been impressively confirmed. Positive EMC tests should be, apart from legal aspects, an important criterion for the chosen hardware and software measures – it simply boils down to this.
Moreover they don't guarantee stable functionality, particularly if interference energies reach the external world weakened by sophisticated case constructions and external screen measures only in order to comply with the respective, legally prescribed upper limits. In return they "rave up" within the assembly, many

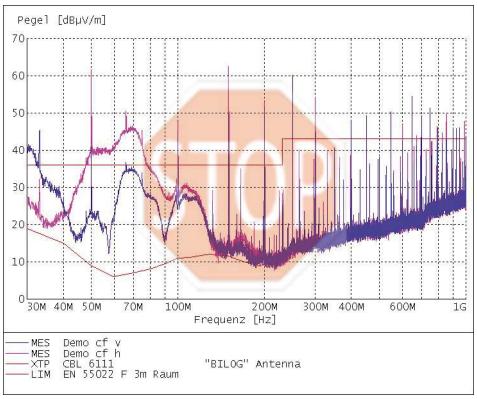


Fig. 6: Interference spectrum in case that physics were not convinced: test object was a standard MCF5407-Coldfire demo board, test-software was the same MCF5407-CPU-SDRAM memory test (clock see figure 7)



Figure 7: Ilk signal forms undermine any system stability: The 50 MHz clock signal "condign" to the MCF5407-Coldfire demo board (the interference spectrum is shown in fig. 6)

a time leading to puzzling instabilities in usually independent functional areas (figures 6 and 7).
A new European EMC guideline with substantially eased regulations has been drafted , which becomes effective at the beginning of 2004: a so called "EMC-law light". As a consequence (result) it will be easier for the manufacturer to obtain and use the CE mark regarding EMC.
Therefore it becomes increasingly important to counter interfering emission and immission in various fields of electronics by constructive measures. The combination of software (CPU) and hardware flexibility (99% of FPGA resources are freely available), the high bandwidth of the input/output structures, the extensive constructional measures in the PCB design, the optimisation strategies within the interrelation of schematic draft and PCB design elaboration (avoidance principle, component selection, piled power planes etc.) are setting new benchmarks regarding stability and functionality [3].
In the long run software with few bugs or being errortolerant can be realized economically on stabile hardware platforms only. *(cm)*

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EMC-compliant design

Function and EMI in Harmony

Finally EMI and functional stability of a system are linked in a way, that without profund EMI measures system stability and function cannot be achieved. The EMC-conform design of a microprocessor board is divided into three areas of provisions. It starts with the selection of low noise components. The second area regards the adequate layout of the power supply distribution systems within the PCB itself. The third area of necessary provisions concerns the layout of the signal-line system

by Prof. Chistian Dirks

The EMC-compliant design of a microprocessor system starts with the selection of low noise components. Those are the ones , which produce the smallest possible di/dt. As such data are practically not yet available from manufacturers, the designer has to find out the EMI-characteristics himself.
The power consumption of the component can provide some initial information. But the comparison on this level is only possible if the integrated circuits show the same speed rates and are quite similar in other aspects of performance too. The comparison by micro-H-probe-measurements [1], [2] is much more promising.
The second area of means to be talen (the second field of tasks) regards the adequate layout of the power supply distribution systems within the PCB itself.
The first aspect is certainly the correct supply of the integrated circuits, the second aspect however is the preferably entire absorption of the electromagnetic energy caused by pulse-shaped current draw. Concerning the above measures taken both aspects have to be considered otherwise the power supply system, in case of a wrong construction, turns out to be the main source of EMI within the PCB and can make the complete system functionally unstable.
The third aspect that has to be dealt with concerns the layout of the signal-line system. Much attention should be paid to the appropriate termination.
The faster the digital systems , the more the transmission-line character of any conductor in the PCB will become evident. Ignoring this fact may lead to a disastrous overall-design of the PCB.
To give an example the EMC relevant details will be considered in the design of a complex industrial PCB below.

Component selection:

The selection of integrated circuits is mainly determined by the desired function. Nevertheless the same function normally can be achieved by different components. Therefore it always pays to analyse suitable components with regard to their EMC-properties. This will be done with the example of the microprocessor used in the PCB in question.
As previously mentioned, the power consumption of an integrated circuit can be, although with restrictions, a certain reference to the EMC characteristics. Energy which is not drawn from the power supply simply cannot be transformed into noise power.
The microprocessor in use is the MC5407; its power consumption rates approx. 500 mW at an internal clock of 200 MHz and 240 MIPS in a considerably normal operating condition. For reasons of comparison only: The consumption of the



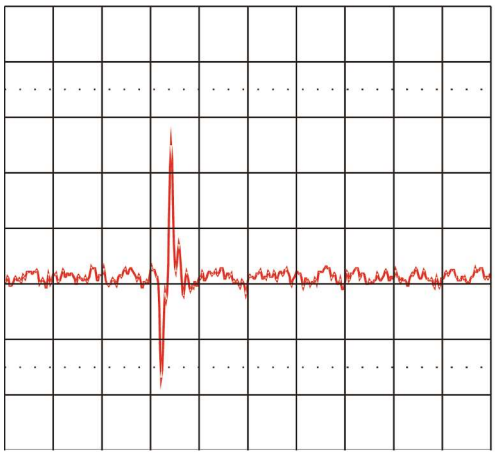


Figure 1:
Micro-H-probe pulse of the MCF 5407: The pulse amplitude amounts to 50 mV showing a low noise element

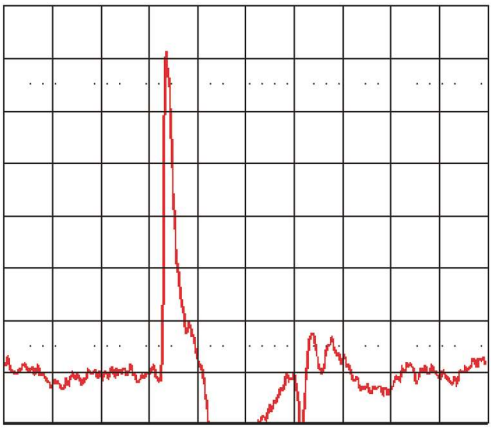


Figure 2:
Micro-H-probe pulse of a noisy IC 68HC000: the pulse amplitude amounts to 300 mV (resolution: 10 ns/20 mV and 10 ns/50 mV)

CPU of a 500-MHz-PC amounts to 8 W. Well, of course this is not a scientific analysis of the problem, however a factor 16 definitely is an interesting aspect. Heat sinks found on digital integrated circuits that come along with heat sinks should make anybody suspicious who is involved in EMC.

Improving a noise level of about 15 dB is expensive

Measurements with a micro-H-probe are much more significant.1]. In both cases a „hot" spot was taken (chosen) on each processor. Figure 1 shows the pulse of the micro-H-probe measured on the CPU (MCF5407) of the PCBconsidered. The pulse amplitude amounts to 50 mV and designates a relatively low noise element. In comparison figure 2 shows the micro-H-probe pulse on a high noise element (68HC000). The pulse amplitude amounts to 300 mV. In this case an approximately 15 dB higher noise level is to be expected.
Ergo: This example clarifies quite well, that the consideration of the EMI characteristics should affect component selection. Improving the noise level of a PCB by other means in a range of about 15 dB usually is troublesome and expensive.
Nevertheless the integrated circuits cannot be selected under EMI aspects only. At least the specified performance has to be provided. In princiole the faster a circuit has to operate and the more tasks have to be performed in parallel the higher the di/dt will be on the power supply system.
Especially in this case the component selection will be critical. On the PCB considered the concerned element is the Virtex-II (XC2V1000-6FG256) (approx. 1 million gates). The micro-H-probe pulse on this integrated circuit is amazingly low, reaching not even 40 mV in full-performance-operation. The circuit therefore has to be considered as low noise, being particularly remarkable regarding its performance.
Noise power can be avoided substantially by clever component selection – however unfortunately not all of it. Regarding high processing power this „remainder" can be really disagreeable. Thus in most cases a careful noise reduc- ▶

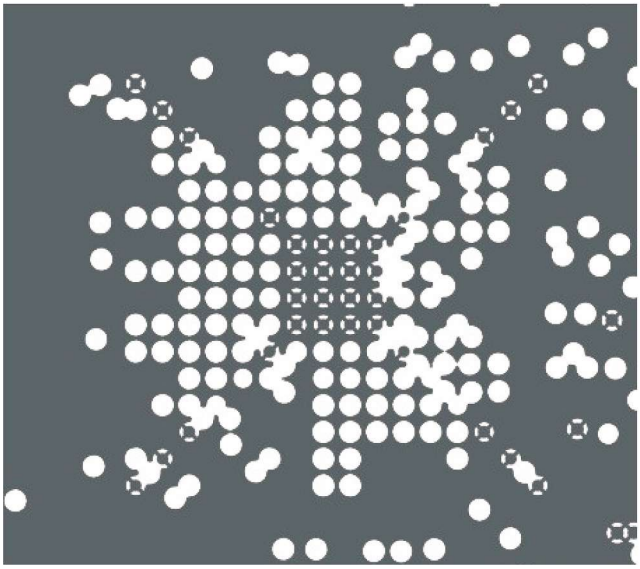


Figure 3: Connection of a VLSI-circuit to the GND-plane; correct implementation of the connections into the GND-plane

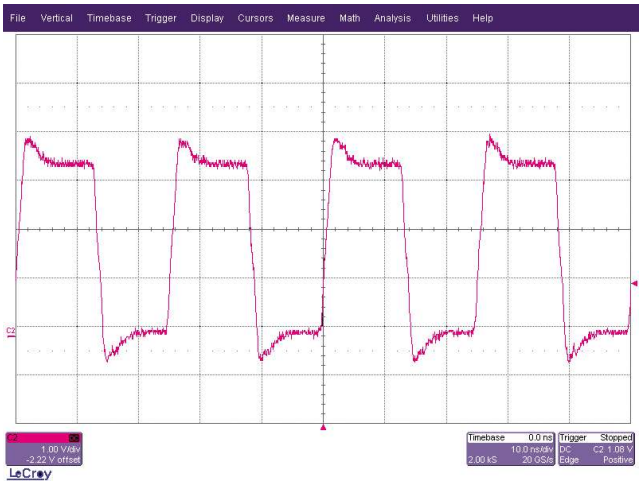


Figure 4: Signal waveform of an active terminated signal line (resolution: 10 ns/1 V); the signal waveform is advantageous regarding EMC and leads to a stable function of the system

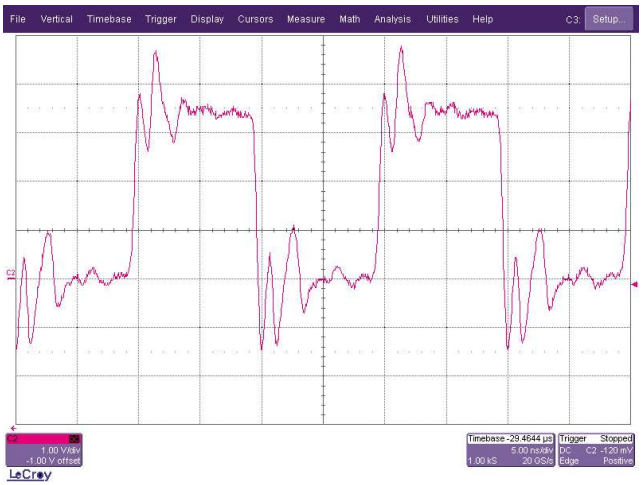


Figure 5: Signal waveform of an unterminated signal line (resolution: 10 ns/1 V); regarding EMC result is bad and even the functionality is endangered, because level limits are violated

tion of the PCB will be necessary even if the components have been selected accurately. Hereby noise reduction is not to be understood as any additional measure on an already finished PCB but as a physically correct construction of it from the very beginning.

Decoupling of the power supply system:

The use of modern VLSI-circuits requests power distribution systems that provide high currents in extremely short times. Due to unsatisfactory decoupling voltage drops in the power supply may reach an amount, so that stable system function cannot be guaranteed anymore. Only for relatively low frequencies the decoupling can be achieved with capacitors.

The reason lies in the fact that capacitors in first approximation behave as series resonant circuits. They are only narrow-band low-impedance and therefore an effective decoupling is only possible in this low frequency range. The frequency range for efficient decoupling with capacitors is extendable by means of building correctly dimensioned capacitor groups [2], [4], that are useful in a frequency range of up to 300 MHz. Above that range power distribution systems are to be implemented as planes. In case of the PCB examined anything else was out of question.

Such plane systems usually consist of a Vcc-plane and a GND-plane separated by an insulating layer of minimum thickness. A distance of 100 microns or less is recommendable (recommended). Considering PCB-dielectrics that are presently available it never should be more than 120 microns. Such a powerplane system has some outstanding characteristics: It is able to carry a considerable electric charge and deliver it to a load in a very short time. At an εr of 4 such a plane area can be discharged at a speed of 15 cm/ns due to the transmission-line characteristics of the plane system [3].

Arrange Vcc- and GND-Planes in an alternating sequence

E.g. for a current pulse of 1 ns duration the required charge has to be found in the radius of 15 cm around the power pin of the integrated circuit. For an approximate calculation of the available charge the formula for plate capacitors should be sufficient. In case the stored charge is insufficient, the substrate thickness between adjacent Vcc- and GND-planes may be decreased. For VLSI-circuits it might be the case, that even this is insufficient because substrates possibly may not be as thin as necessary. Asking for a 20 micron substrate would cause fierce opposition from most of the PCB manufacturers.

Much more charge can be provided by plane systems if the planes are piled, Vcc- and GND-planes are arranged in an alternating sequence.

By means of such piled Vcc/GND systems even a large di/dt can be handled. Anyhow, it has to be considered that this functionality is only achieved if the Vcc- and GND-pins of the integrated circuit are directly connected to the plane system. Figure 3 shows the correct connection of a VLSI-circuit to the GND-plane. The thermal pads are tolerable without any problems. This type of connection should also be used for all piled GND-planes. This procedure accordingly applies to Vcc planes as well. Low-frequency components within spectra of long pulses can be covered by capacitors in the low-band range or by capacitor groups in the broad-band range. They have to be calculated by taking the plane properties into consideration[4]. The capacitor group is placed on the back(side) directly under the integrated circuit and connected straight into the planes.

After having exemplified how to provide a suitable power supply system for VLSI-circuits even in case of critical current load, the second aspect of power distribution systems shall be taken into account: EMC.
Considering EMC guide-lines the transport of electro-magnetic energy should always happen in strictly bounded areas. Concerning PCB's it can be achieved when current and reverse-current are kept close together. In a plane power supply system this requirement is practically fullfilled in a perfect way.
Additionally there's a second aspect: In a transmission line prone to losses, the losses increase by a decreasing characteristic impedance of line. E.g. the λ/4-resonance of a short-circuited plane system within a PCB tops at a maximum impedance of approx. 2 Ω at 60 micron substrate thickness. The piled power supply system in the PCB considered resembles the parallel circuit of 5 of the above described systems – but with a substrate thickness of only 50 microns, which means that no considerable resonance peak is to be expected. Basically the system is anechoic. On the other hand it means that the electromagnetic energy is absorbed to greatest possible extent within the conductor losses. This is the reason why correctly dimensioned power plane systems are outstandingly advantageous regarding EMC. [2].

Cleaning up of the signal line system:
Any signal power fed into a transmission line appears as interference power after completion of the data-transmission. We do need the power for the transmission of the information. Unfortunately it doesn't disappear after the information is transmitted. So we have to provide for the absorption of this power at the end of the signal line. Such kind of precaution is named termination. It converts arriving signal energy into heat and causes thereby the desired anechoic behaviour of the transmission line.
The basic procedure is well known from high-frequency engineering. However, regarding digital systems the situation is different so that the methods practically cannot be transferred. E.g. the input of a digital circuit is, considering its broadband behaviour, a complex frequency-dependent load. Nevertheless it has to be terminated merely resistively with the characteristic impedance of the line. For single mono-directional lines there are definitely solutions. But regarding lines ending on several inputs of digital circuits these solutions do not work anymore.
The approach concerning digital systems therefore is different: The reflection-caused under- and overshots at the line ends are limited and a considerable part of the noise energy is absorbed right at the origin. One of the known possibilities is the Schottky-termination.The functional principle is first to connect a diode between signal line and power supply, which will be conductive if the signal voltage exceeds the supply voltage. Second, a diode between signal line and GND is connected, which conducts if the signal voltage falls below the GND potential. Unfortunately the disadvantage of this solution is that in each way the threshold voltage of the diodes has to be overcome. E.g. in a 3-V-system the 0.8 V of common silicon diodes virtually shoot the effect down.

All signal lines have been actively terminated

A more convenient answer to the problem are active termination chips, available as integrated circuits. They don't show threshold voltages. Both solutions rely on a stable Vcc/GND system provided along with the signal lines. If this condition is not fulfilled even active terminations do not work. Due to failures resulting from lousy Vcc/GND systems unfortunately even good termination circuits have been discredited.
In case of the PCB in question all signal lines have been actively terminated using the PI7AT04 of Pericom [5].
Figure 4 shows the signal waveform of an actively terminated signal line. It is advantageous regarding EMC and yields a stable function of the system. In comparison figure 5 shows the signal waveform on a line without termination. The signal has been measured on a commercially available demo board. Regarding EMC the result is unsatisfying and even the functionality is jeopardised because level limits are violated so that a stable function of the system may not be expected. Finally EMI and functional stability of a system are linked in a way that without profund EMI measures system stability and function cannot be achieved.
Through this example it can be clearly seen how EMI measures and system stability are linked in state of the art digital systems. Without a good EMC often also the stable function cannot be ensured.

PCB layer stack-up:
The previous remarks find their conclusion in the EMI- correct layer stack-up of the PCB (figure 6). The following principle

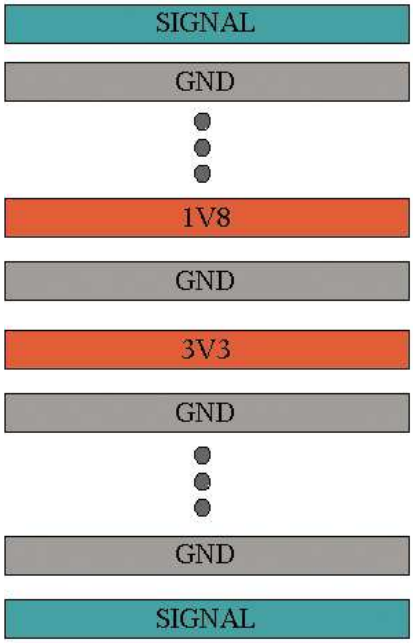


Figure 6: EMC-correct – schematical representation of the PCB layer stack-up

is to be implemented: For each signal layer and each Vcc-layer an adjacent plane layer (preferrably GND) is necessary to carry the reverse currents.
The schematic representation of the layer stack-up in figure 6 not only meets this requirement. The core of the board is given by the piled Vcc/GND system for the different supply voltages, consisting of Vcc-layers for 3.3, 1.8 and 1.5 V and their respective GND-layers. Each of the eight signal layers also holds an adjacent GND-plane.
Altogether an 18-layer board was the result.This represents a massive effort! Nevertheless the result is remarkable: The EMC-certification with a safety margin of 10 dB has been awarded in the first attempt (has been immediately awarded) and the system is absolutely stable, a property not to be underestimated, because unstable systems (systems weak in function) usually cause severe problems. *(cm)*

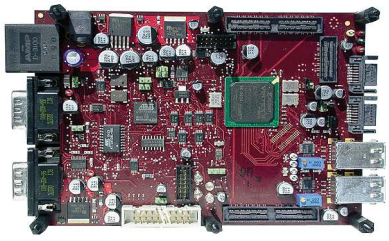
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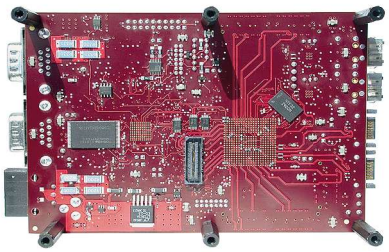
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Hardware meeting requirements of tomorrow

Characteristics of “meltemi”

The “meltemi”-platform is designed for image processing, HDTV or digital video and TV applications, a field where loads of data have to transmitted. An effective 20-layer stack-up with integrated power supply sequence, impedance controlled trace routing, X2Y-capacitors and edge plating allows transmission bandwidth up to 60 Gbit/s associated with excellent EMC behaviour and maximum functional stability and operational reliability as measurements in the EMC laboratory prove. The multilayer stack-up of “meltemi” fulfils four requirements securing the reliable function of the device: 1. Decoupling, 2. EMC-immission/ -emission, 3. Signal integrity and 4. Self interference.





In the second part of the “meltemi” project the reference hardware platform “meltemi economic” – a 6-layer board with 32-bit single chip multicontroller was developed. Flexible I/O structure and free programmable hardware accelerators or re-programmable logic extend the life circle of the hardware.

To fulfil the four requirements in this project as well the followings tasks among other had to be solved:

- Broadband decoupling of four power supply systems, that means only two remaining layers for signal routing
- Partitioning into two symmetrical inside lying power supply system layers with both signal layers on each external layer,

decoupling each power pin both of the ARM7-CPU and the Spartan-3-FPGAs by chokes with respective ohmic resistance, impedance controlled signal routing, capacitor groups, edge plating and edge capacitors.

The approach leads to construction rules and operational strategies for future circuits.

Anybody interested in putting these expenditure of time aside or interested in experimentation can purchase the complete platform inclusive of the documentation with schematic and PCB-design at unit^el. Contact: Gerhard Eigelsreiter.

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